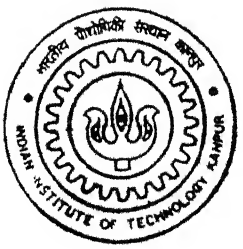
STUDY OF 3GPP WCDMA (FDD) DOWNLINK FOR SOFTWARE CONFIGURABLE RADIO BASE STATION SYSTEMS

by

BELLAM SASI KUMAR



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STUDY OF 3GPP WCDMA (FDD) DOWNLINK FOR SOFTWARE CONFIGURABLE RADIO BASE STATION SYSTEMS

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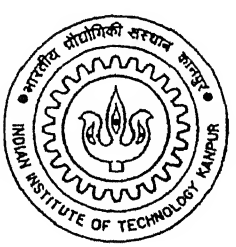
Bellam Sasi Kumar



to the

Department of Electrical Engineering
Indian Institute of Technology, Kanpur
February 2001

CERTIFICATE

This is to certify that the work contained in the thesis entitled **STUDY OF 3GPP WCDMA (FDD) DOWNLINK FOR SOFTWARE CONFIGURABLE RADIO BASE STATION SYSTEMS** by **Bellam Sasi Kumar** (Roll No 9910422) has been carried out under my supervision and that this work has not been submitted elsewhere for any degree or diploma.

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Dedicated to

My parents and Sister

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Sasi Kumar

Abstract

First and second generation cellular systems are optimized for voice traffic. Present generation cellular base stations use dedicated hardware to realize physical channels. They employ a bank of narrow band transceivers one for each channel. The cost/complexity of these base stations grows linearly with the number of supported channels. Also, seamless global roaming in multi-standard environments is not supported by the present generation system. In contrast, software radio/virtual radio approach provides reconfigurability of the system. In this approach all physical channels are realized using software modules that run on a processing platform with wideband ADC at front end. The ADC digitizes the whole service RF band for subsequent software processing. In strict sense software radio uses Digital Signal Processors (DSPs) while virtual radios uses general-purpose processors for software processing of digital bit stream from the ADC. The advantages of software only approach are numerous such as support of global roaming in multi-standard environments, ease in upgradation as it eliminates the need to replace the dedicated base station hardware etc. However, the difficulty in the software-approach realization of a cellular system is the requirement of high dynamic range wideband ADCs as well as heavy processing power requirements for software processing of bit streams.

The goal of next generation mobile communications system popularly called as Third Generation (3G) Cellular Systems, is to seamlessly provide a wide variety of communication services such as high speed data, video and multimedia traffic as well as voice traffic. One of the most promising air interface that is accepted worldwide that meets 3G requirements is the Wideband Code Division Multiple Access (WCDMA).

In the present work we have focused on processing power requirement part of the software-only approach and have studied the feasibility of realization of 3G WCDMA base station systems in software. We have assumed virtual radio environment for our work. Using C language we have realized all downlink physical channels for FDD mode of 3GPP WCDMA base station system according to physical layer specifications of the 3GPP group. Each downlink physical channel is realized by implementing all its physical layer operations such as CRC coding, channel coding, rate matching, interleaving,

spreading and scrambling in software. By executing all the above operations for each downlink physical channel on a general purpose processor (virtual radio approach) the computational power required to realize each downlink physical channel has been estimated and expressed in terms of %CPU metric and in terms of SPEC ratings. As the computational power expressed in %CPU metric depends on the processor used, SPEC ratings are used to express the computational power in a processor independent way Three base station systems each with different downlink channels are assumed and computational power required to realize the whole downlink of each system has been evaluated. From the computational requirements of each of the assumed base stations, a figure of computational power requirement for downlink in practical real time base stations has been estimated. From the results obtained in our work, we observe that the virtual radio approach is quite attractive but the realization cannot be supported by the computational power of present day processors.

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List of Abbreviations

3GPP	:	3rd Generation Partnership Project.
ADC/DAC	:	Analog to Digital / Digital to Analog converter.
AI	:	Acquisition Indicator.
AICH	:	Acquisition Indicator Channel.
AMR	:	Adaptive Multi rate
AP-AICH	:	Access Preamble Acquisition Indicator Channel
API	:	Acquisition Preamble Indicator.
ARIB	:	Association for Radio Industry and Business
AS	:	Access Slots.
ASIC	:	Application Specific Integrated Circuit.
BCH	:	BroadCast Channel.
BS	:	Base station
BPSK	:	Binary Phase Shift Keying.
CAI	:	Channel Assignment Indicator.
CC	:	Convolutional Code.
CCTrCH	:	Coded Composite Transport Channel.
CD/CA-ICH	:	Collision Detection/Channel Assignment Indicator Channel.
CDI	:	Collision Detection Indicator.
CDMA	:	Code Division Multiple Access
CPCH	:	Common Packet Channel.
CPICH	:	Common Pilot Channel.
CPU	:	Central Processing Unit.
CRC	:	Cyclic Redundancy Check.
CSICH	:	CPCH Status Indicator Channel.
DCH	:	Dedicated Channel.
DCCH	:	Dedicated Control Channel.
DPCH	:	Dedicated Physical Channel.
DPCCH	:	Dedicated Physical Control Channel.

DPDCH	:	Dedicated Physical Data Channel.
DS-CDMA	:	Direct Sequence Code Division Multiple Access.
DSP	:	Digital Signal Processor.
DTX	:	Discontinuous Indication.
ETSI	:	European Telecommunications Standards Institute
FACH	:	Forward Access Channel.
FDD	:	Frequency Division Duplex.
GHz	:	Giga Hertz.
GSM	:	Global System for Mobile communications.
GuPPI	:	General Purpose Peripheral Component Interconnect Interface.
HSN	:	High Speed Network.
ICH	:	Indicator Channel.
IF	:	Intermediate Frequency.
ISDN	:	Integrated Digital Services Network.
Kbps	:	Kilobits per second.
Ksps	:	Kilo symbols per second.
MAC	:	Medium Access Control.
Mbps	:	Mega bits per second.
Mcps	:	Mega chips per second.
MDNS	:	Multi DSP Network Structure.
MDTS	:	Multi DSP Tree Structure.
MHz	:	Mega Hertz.
OVSF	:	Orthogonal variable Spreading Factor.
PCCC	:	Parallel Concatenated Convolutional Code.
PCCPCH	:	Primary Common Control Physical Channel.
PCH	:	Paging Channel.
PCPCH	:	Physical Common Packet Channel.
PDSCH	:	Physical Downlink Channel.
PhCH	:	Physical Channel.
PI	:	Paging Indicator.
PICH	:	Paging Indicator Channel.

PRACH	:	Physical Random Access Channel.
PSC	:	Primary Synchronisation Code.
P-SCH	:	Primary Synchronisation Channel.
PU	:	Processing Unit.
QPSK	:	Quadrature Phase Shift Keying
RACH	:	Random Access Channel.
RF	:	Radio Frequency.
RLC	:	Radio Link Control
RM	:	Rate Matching.
RRC	:	Radio Resource Control.
SCH	:	Synchronisation channel
SCCPCH	:	Secondary Common Control Physical Channel.
SF	:	Spreading Factor.
SI	:	Status Indicator.
SPEC	:	Standard Performance Evaluation Corporation
SSC	:	Secondary Synchronisation Code.
S-SCH	:	Secondary Synchronisation Channel.
SWR	:	SoftWare Radio.
TC	:	Turbo Code.
TFCS	:	Transport Format Combination Set.
TDD	:	Time Division Duplex.
TFCI	:	Transport Format Combination Indicator.
TPC	:	Transmit Power Control.
TrBK	:	Transport Block
TrCH	:	Transport Channel.
TTI	:	Transmission Time Interval.
UE	:	User Equipment.
UMTS	:	Universal Mobile Telecommunication System.
UTRA	:	UMTS Terrestrial Radio Access.
UTRAN	:	UMTS Terrestrial Radio Access Network.
WCDMA	:	Wideband Code Division Multiple Access.

Chapter 1

Introduction

The goal of the next generation mobile communication system is to seamlessly provide a wide variety of communication services to anybody, anywhere at anytime. The intended service for next generation mobile phone users include services like transmitting high speed data, video and multimedia traffic along with the usual voice traffic. The technology needed to tackle the challenges to provide these services is commonly known as the Third Generation (3G) Cellular Systems [1].

The first generation cellular systems were represented by analog mobile systems designed to carry the voice traffic. Their subsequent digital counterparts are known as the current second generation cellular systems. Third generation cellular systems mark a significant leap, both in applications and capacity from the present second generation cellular systems. While the current digital mobile phone systems are optimized for voice communications, third generation systems are oriented towards multimedia message capability.

To enable the global and seamless roaming of mobile users third generation cellular systems must feature a high degree of flexibility and adaption even at the physical layer. For this purpose radios with software reconfigurable functionality in every architectural layer are considered essential components of third-generation systems.

1.1 Concept of Software radios and Virtual radios:

In past programmable radios used some general purpose processor for most of the functions, but left the computationally intensive radio functions to ASIC or DSP devices. Improvements in processor technology made it possible to realize all the radio functions in software, known as software radios [2] or virtual radios [3].

Calling the approach of software radios and virtual radios as software based approach, they are realized as follows. Software based approach [4] contains a wideband ADC/DAC at Radio Frequency (RF) front end to sample and digitize the entire serving

RF band. From the digital output from ADC individual frequency channels are extracted, all channels are down converted from passband to baseband and base band processing is done, all in digital domain. All these operations on data bits are performed by software modules that run on a processor. Software radios and Virtual radios are differentiated by the processing platform on which these software modules are executed. Software radios use Digital Signal Processors (DSPs) whereas Virtual radios use general purpose workstations/PCs to run software modules for processing the digital streams.

In case of base stations (BSs), software based BSs have many advantages compared to conventional hardware based systems. Conventional base stations use dedicated hardware for each RF channel associated with complete receiver chain including RF amplifier, filters, demodulators whereas software based BSs uses single wideband RF front-end with one wideband ADC. Bits from ADC are processed, channels are extracted and further processing are done in software [5], [6]. The use of single RF front end drastically reduces the cost of the base station. In case of base station upgradation for enhanced services or to a new standard, there is no need to replace partial or complete hardware. In such cases software based BS need only software upgrade or replacement, which can be done with ease. And for subscribers software based approach provides easier international roaming, improved and more flexible services. For BS manufacturers, software based approach provides increased production flexibility and improved product evolution.

However, software based BSs has many difficulties in their realization [7]. Also in mobile environments dynamic range of received signal varies much from near end user to far end user needing high dynamic range wideband ADC/DAC, which are difficult to achieve at the present level of hardware technologies. Another major difficulty in the realization of software based BSs is the requirement of high computational power for software processing of the digital stream. Much more details of software radios can be seen in [8].

1.2 Third Generation Cellular Systems

Third generation (3G) cellular systems are supposed to support wideband services like high speed Internet access, video and high quality image transmission with the same

quality as the fixed networks. The main requirements of the third generation cellular systems are:

- Minimum data rate of 144 kb/s for full coverage and vehicular mobility, and 384 kb/s for pedestrian mobility.
- 2 Mbps data rate for limited coverage and mobility (e.g. indoor office).
- Support of packet switched data services.
- High spectrum efficiency (more users) compared to existing systems.
- Support of a wide variety of mobile equipment
- Backward compatibility with the existing networks and high flexibility to introduce new services and technology
- An adaptive radio interface suited to the highly asymmetric nature of most Internet communications: a much greater bandwidth for the downlink than the uplink.

1.3 Air Interface for 3G

In the search for most appropriate multiple access technology for 3G systems, a number of wideband CDMA schemes have been proposed [9]. Among them Wideband CDMA (WCDMA) [10] and CDMA 2000 are the two most popular schemes. WCDMA is a network asynchronous scheme while CDMA 2000 is network synchronous scheme. In network asynchronous scheme the base stations are not synchronized using a common clock, while in the network synchronous schemes the base stations are synchronized to each other within a few microseconds. WCDMA used single carrier and CDMA 2000 uses multi carrier that is motivated by a spectrum overlay of cdma2000 with existing IS-95 carriers.

The nominal bandwidth for all third-generation proposals is 5 MHz. There are several reasons for choosing this bandwidth. First, data rates of 144 and 384 Kb/s are achievable within 5 MHz bandwidth for third-generation systems and can be provided with reasonable capacity. Even 2 Mbps peak rate can be provided under limited conditions. Second, lack of spectrum calls for reasonably small minimum spectrum allocation, especially if the system has to be deployed within the existing frequency bands already occupied by the second generation systems. Third, the large 5 MHz bandwidth can resolve more multipaths than a narrower bandwidth, thus increasing

diversity and improving performance. Larger bandwidths of 10, 15, and 20 MHz have been proposed to support highest data rates more effectively.

Following section presents a brief discussion on WCDMA.

1.3.1 WCDMA

The WCDMA scheme has been developed as a joint effort between ETSI (European Telecommunication Standard Institute) and ARIB (Association for Radio Industry and Business) and is commonly known as UTRA (Universal Mobile Telecommunication System Terrestrial Radio Access) The access scheme for UTRA is Direct-Sequence Code Division Multiple Access (DS-CDMA) with information spread over approximately 5 MHz bandwidth, thus often denoted as wideband CDMA [11].

The key operational features of the WCDMA radio interface are

- Support of high data rate transmission: 384 Kbps with wide area coverage, 2 Mbps with local coverage.
- High service flexibility: support of multiple parallel variable rate services on each connection.
- Both Frequency Division Duplex (FDD) and Time Division Duplex (TDD).
- Built in support for future capacity and coverage enhancing technologies like adaptive antennas, advanced receiver structures and transmitter diversity.
- Support of inter frequency hand over and hand over to other systems, including hand over to GSM.
- Efficient packet access.

As WCDMA provides data transport services, which are asymmetric in nature and as the requirement is also to support transmission in unpaired bands in some regions, TDD mode was included in WCDMA in addition to FDD mode. In FDD mode a physical channel is specified by specific frequency and spreading code while in TDD mode the physical channel is specified by the frequency, spreading code and timeslot. In WCDMA data is transmitted in frames of 10 ms duration. Each 10 ms radio frame is divided into 15 slots with 2560 chips/slot at the chip rate 3.84 Mcps. The information rate of the channel varies with the symbol rate being derived from the 3.84 Mcps chip rate using channelisation code of variable length (variable spreading factor) called as Orthogonal

Variable Spreading Factor (OVSF) code. OVSF codes are generated by using tree structure as given in Chapter 3.

Following table shows the key technical features of the WCDMA radio interface.

Table 1.1: Key features of the WCDMA radio interface

Multiple Access Scheme	DS-CDMA
Duplex Scheme	FDD/TDD
Channel bandwidth	5 MHz
Chip Rate	3.84 Mcps
Carrier Spacing	4.4-5.2 MHz
Frame Length	10/20/40/80 ms
Inter Base Station synchronization	FDD: No accurate synchronization needed TDD: Synchronization required
Multi rate	Orthogonal Variable spreading factor codes and multiple code
Spreading factors	4-256(Uplink) 4-512(downlink)
Channel Coding Scheme	Convolutional code (rate 1/2 and 1/3) Turbo code
Data modulation	QPSK(downlink) BPSK(uplink)
Spreading (downlink)	Variable length orthogonal sequences for Channel separation, Gold sequences of length 2^{18} for cell and user separation (truncated over cycle of 10 ms)
Spreading (uplink)	Variable length orthogonal sequences for channel separation, Gold sequence of length 2^{41} for user separation (different time shifts in I and Q channel, truncated cycle 10 ms)
System timing	Network asynchronous

Spreading factor varies from 256 to 4 for FDD uplink, from 512 to 4 for FDD downlink and from 16 to 1 for TDD uplink and downlink. Thus the respective modulation symbol rates vary from 960 k symbols/s to 15 k symbols/s (7.5 k symbols/s) for FDD uplink (downlink), and for TDD the momentary modulation symbol rates shall vary from 3 84 M symbols/s to 240 k symbols/s. In downlink Gold sequences of length 2^{18} truncated to form a cycle of 10 ms frame are used for scrambling. In uplink long codes and short codes are used for scrambling. Short codes are Kasami sequences of length 256 and long codes are Gold sequences of length 2^{41} but truncated to form a cycle of 10 ms frame. The chip rate may be extended to two or three times the standard 3 84 Mcps to accommodate for data rates higher than 2 Mbps. The 200 kHz carrier raster has been chosen to facilitate coexistence and interoperability with GSM

1.4 Objective of the thesis:

First and second generation cellular base stations use dedicated hardware and employ a bank of narrow band receivers, each having its own complete receiver chain for each channel. The cost/complexity of these base stations grows linearly with the number of channels supported. Also, this approach cannot provide seamless global roaming in multi-standard environments. The whole base station hardware would need replacement in case of upgradation to new standard. In contrast, the software based approach provides global roaming, reduction of cost by using single wideband receiver and ease in upgradation to a new standard that eliminates the need of replacing the whole base station hardware. The main challenge in realization of software only approach is the requirement of high dynamic range wideband ADC's and high computing power required for software processing of radio function modules. We study realization of the software configurable radio base station systems for WCDMA (FDD). Focusing on the computational power requirement part, in this thesis, the computational power required for realizing all the downlink channels in a typical WCDMA (FDD) base station was investigated and corresponding requirement of the computational power was estimated.

1.5 Organization of the thesis:

Chapter 2 describes the concept and advantages of software and virtual radios in detail. Chapter 3 and 4 explains the downlink channels and their structure as well as the physical

layer details of WCDMA system. Chapter 5 describes the implementation details of downlink physical channels. Chapter 6 gives the computational power required to realize all downlink channels and concludes the study with scope outlining for future work.

Chapter 2

Software Radios and Virtual Radios

2.1 Software Radios

In its original form, the term Software Radio refers to reconfigurability of the radio interface by software, possibly using the over-the-air download, with an implicit assumption of analog-to-digital conversion as close to the antenna as possible, as shown in Fig.1. As already stated it consists of a wideband ADC to sample and digitize the incoming RF signal followed by processing platforms (DSP/Workstation/PC) for software processing of the resultant digital signal. The generic architecture shown in Fig.1 applies to handsets and as well as base stations.

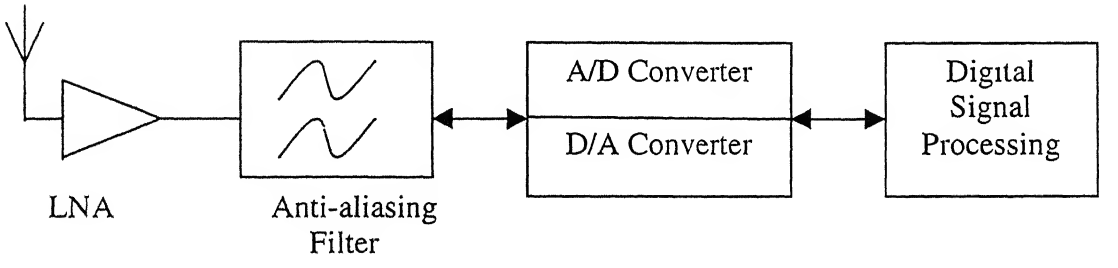


Figure 2.1: Generic Software radio architecture

The main challenge in realization of above architecture is the requirement of high dynamic range wideband A/D/A converter at RF (near far ratio in WCDMA could be around 90 dB) and high processing requirement for the sampled digital signal.

In order to realize such ADC requirements, a few techniques have been proposed, including division of whole receiving band into many sub-bands and utilization of several parallel ADCs, one for every subband [12]. Another possible method is to control or suppress the signal's dynamic range at the input of ADC by application of a logarithmic compression of the signal before digitization and subsequently performing a digital anti-log processing to restore the original signal properties [13]. A further new possible approach to suppress the high dynamic range of the signal at the input of ADC has been given in [14].

Following the ADC, the processing domain in the architecture illustrated in Fig.1 should be capable of processing the digital data produced by the ADC and apply software means to implement a number of radio functions in real time The main question arising in this context again concerns the type of processing domain (DSP or General purpose CPU) and structure of processing domain. As stated earlier Software Radio uses DSP's and Virtual Radio uses General Purpose CPU's for signal processing. In simplest case, the processing domain could just be a single processor (DSP or CPU); however, it is not likely that a single processor could satisfy all the performance requirements for base station systems.

A straight forward yet powerful approach to get around the processing challenge in base stations is by means of multi-processor structures. In such structures, the overall functionality is distributed among a number of individual processors. The two possible structures of distributed signal processing are multi-DSP tree structure and multi-DSP network structure, as explained below [15]. The first one is based on signal-flow (conventional) approach whereas the second one is based on functional approach with each unit doing a particular function for the entire system.

Multi – DSP Tree structure (MDTS): In MDTS the functionality of processing domain is successively decomposed into a number of individual elements as shown in Figure 2.2. The first decompositional level is mainly channel wise, that is, every branch following an IF processing stage is usually dedicated to the processing of one channel. For every branch, there is an IF processing stage that usually incorporates a filter to select a particular channel and a down sampling process for frequency conversion to baseband. The channel-wise decomposition is based on the assumption that every channel processing can be implemented independently from the other channels. The subsequent decomposition levels are usually based on individual characteristics of each channel depending on baseband processing requirements. This is analogous to the present schemes of demodulation of conventional multi carrier system.

The primary advantage of MDTS is its simplicity. However MDTS cannot easily meet the flexibility requirements of a Software Radio (SWR) base station. This is because each channel is constructed in accordance with the specifications of a particular type of channel and therefore the capacity of MDTS is limited to a given set of channel types.

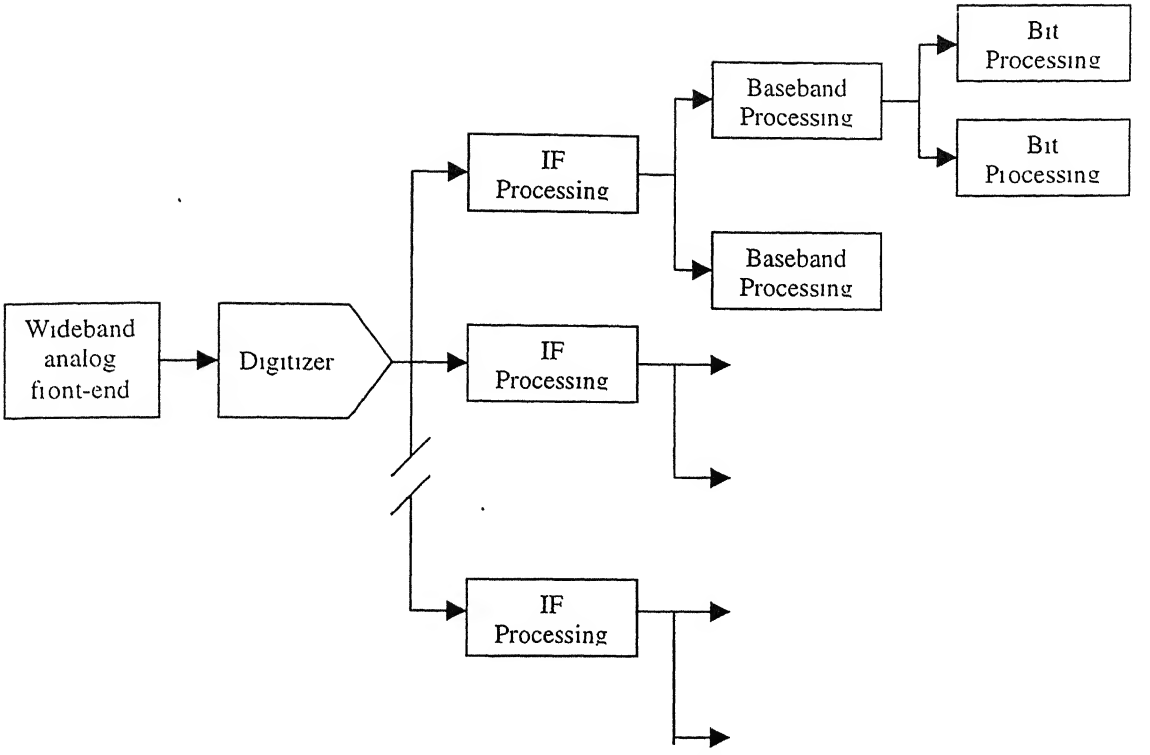


Figure 2.2: Multi – DSP tree structure

A second and more flexible approach is

Multi – DSP Network Structure: Recent advances in memories and processor technology have made it possible to extend the role of the computers to software-based processing of sampled signals. Commercially available processors can process instructions at two or three instructions in a cycle. Therefore, PC- like configurations incorporating two to four advanced processors may have the capacity to perform extensive processing of wideband signal streams. In addition to the advanced processing capabilities, recent workstations can support fast memory – to – memory transfer rates and fast I/O rates. For this reason, several researchers worldwide have recently considered the approach of using general-purpose computers to implement Virtual Radios. An introduction of Virtual Radios is presented in the next section.

The use of general-purpose platforms to implement software radio (SWR) base stations has also been recently considered. Such software implementations have the potential of offering the benefits of SWR architectures, such as great cost savings, by using one transceiver per base station instead of one per channel, tremendous flexibility, reconfigurability, and multistandard support. Due to high complexity and wider

bandwidth, an SWR base station for the third generation high capacity systems cannot be built on a single general purpose workstation but on systems with distributed architectures. A distributed processing architecture for consideration could be a Multi DSP network structure (MDNS), that is, a structure with a number of distributed processing units interconnected by means of a high-speed network Such structures have the potential to satisfy the high requirements of wideband SWR base stations and to provide multistandard, multi-channel operation and instant reconfiguration to support new applications on demand.

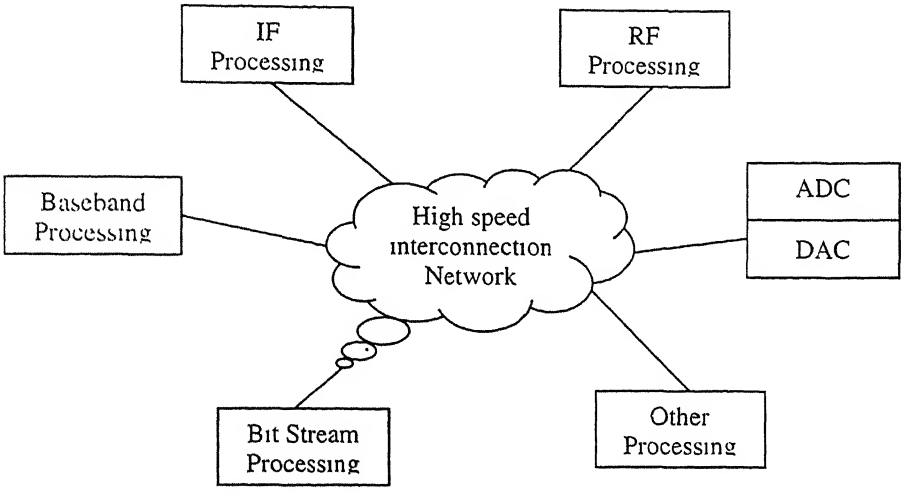


Figure 2.3: Multi – DSP network structure

The basic MDNS approach is illustrated in Fig.2.3. In this new approach, there are number of individual processing units (PUs) interconnected by a high-speed network (HSN). Each processing unit will be a general-purpose processor (Workstation/PC). They may include any kind of processing required in an SWR base station such as IF processing, baseband processing, vocoders etc along with appropriate ADCs.

For example, in a simple operating scenario, the ADC PU digitizes a wideband received signal and forwards the digital data in form of packets to the IF PU via HSN. Once the packets are switched to the IF PU, the channelization of the wideband signal is performed. The individual channel streams generated by the IF PU are routed to the right baseband PU based on type of each stream. For instance GSM channel streams could be sent to a GSM baseband PU, whereas UMTS channel streams could be routed to UMTS baseband PU. After baseband PU, individual channels can be routed to other PUs for

further processing. Following table gives a brief summary of most important advantages of MDNS.

Table 2.1: Advantages of MDNS

Advantage	Comments
Flexibility	Any processing unit can be added, removed or configured without affecting the other processing units. Easy reconfiguration by software means.
Scalability	With more need of processing for supporting increased number of users, more PUs can be added in a transparent way to the system in parallel with the old PUs to improve the overall processing capabilities.
Maintenance	Every processing unit can be tested or adjusted independently, so any possible problems in the system can be located easily and fixed fast.

2.2 Virtual radios

As outlined earlier, Software Radios use digital signal processors (DSPs) for signal processing while Virtual Radios use workstation/PCs instead of DSPs for signal processing. Virtual radios perform wideband digitization of incoming RF signal, then performs the entire digital signal processing in user space on a general-purpose workstation. Thus, a Virtual Radio is a communications device that performs its entire digital signal processing in user space on an off-the-shelf workstation.

The advantages of using general-purpose workstations for digital signal processing rather than DSPs are as follows:

- *Rapid deployment:* Users can easily deploy new devices or append enhancements to existing devices in the same manner in which they currently upgrade device drivers and software, for example, as a self-extracting archive downloaded from an ftp site.
- *Experimentation:* There is a large and growing gap between the capabilities and programming environments available on general purpose workstations and those available on specialized DSP hardware. Implementing the signal processing on the workstation makes it easier to experiment with new algorithms and protocols.

- *Multipurpose Devices:* People are increasingly dealing with multiple wireless communication devices. They have both a cellular modem and a wireless Ethernet for their notebook computer. While multipurpose DSP devices are becoming increasingly available, they can only perform a relatively small number of predefined functions. In virtual radio approach, one adds devices merely by downloading the appropriate software.
- *Integration with other applications:* It is often the case that functionality provided by a radio device is only a small part of a larger application. The functionality provided by a wireless modem, for example, is only a part of what is needed for a network interface. Virtual radios allows one to blur the line between the radio and the rest of the application, thus allowing improved functionality and end-to-end efficiency.
- *Improved Functionality:* Performing all of the signal processing in modular software permits not only the dynamic assignment of channel locations and channel widths, but also of the modulation and coding used on each channel. This allows for the construction of heterogeneous systems that employ different communication standards on different channels. This mechanism can be used to accelerate the migration to new standards.

As current ADC technology and available processors will not support the direct sampling of wide RF bands, Virtual Radio uses a multiband hardware front-end to convert the desired RF band to the IF frequency. Then the wideband IF waveform is sampled and these samples are transferred into host memory by using direct memory access (DMA) using general purpose PCI interface (GuPPI) [3]. The main difficulty in the realization of virtual radios is the requirement of high computational power.

In our thesis we have considered the approach of Virtual Radios and estimated computational requirements for downlink channels of WCDMA (FDD) base station by implementing the baseband processing modules of WCDMA (FDD) downlink channels according to physical layer specifications of 3GPP group [16].

Chapter 3

WCDMA physical layer – Description of physical layer channels (FDD)

This chapter and next chapter gives description of physical layer (layer 1) of the radio access network of a WCDMA system operating in the FDD mode This chapter explains the structure of physical channels of WCDMA system.

3.1 General description of layer 1

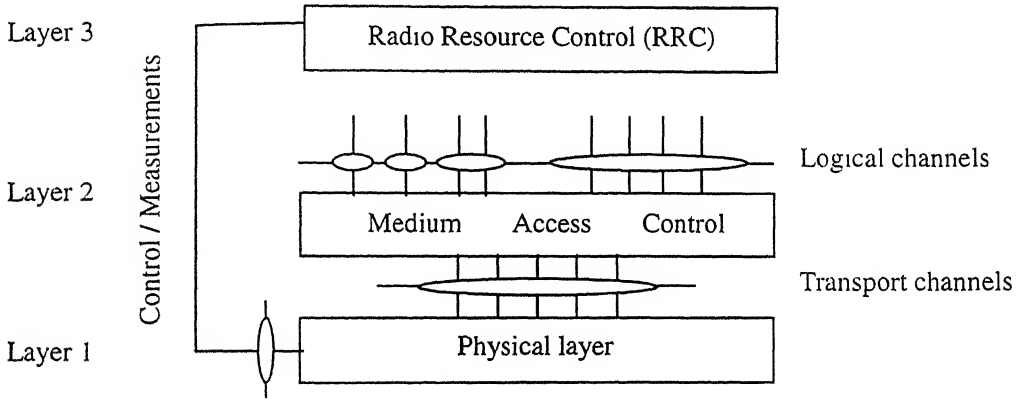


Figure 3.1: Radio interface protocol architecture around the physical layer

Figure 3.1 shows the UTRA radio interface protocol architecture around the physical layer. The Medium Access Control (MAC) sub layer interfaces the physical layer and the Radio Resource Control (RRC) Layer. The physical layer is controlled by RRC. Data from higher layers arrives to MAC layer on logical channels. A logical channel is characterized by the type of information transferred. Radio Link Control (RLC) layer above MAC defines logical channels. MAC delivers data to physical layer through transport channels. A transport channel is characterized by how the information is transferred over the radio interface. Physical channels are defined in the physical layer. Physical layer is based on WCDMA technology. Physical layer maps transport channels onto physical channels. By using its physical channels physical layer provides

transmission of data of transport channels of MAC. A physical channel can be dedicated to a particular user or different users can share it.

3.2 Transport channels

Transport channels are mechanisms through which services are offered by physical layer to/from the higher layers. General concepts about transport channels are described in [17]. We describe them below for a quick reference.

Transport channels in general, can be classified into two groups.

- Dedicated channels, using inherent addressing of User equipment (UE).
- Common channels, using explicit addressing of UE if addressing is needed.

3.2.1 Dedicated transport channels

There exists only one type of dedicated transport channel, the Dedicated Channel (DCH).

DCH - Dedicated Channel

The DCH transport channel exists in both uplink and downlink. Speech data or dedicated data generated at higher layers are mapped onto this channel. The DCH is transmitted over the entire cell or over only a part of the cell.

3.2.2 Common transport channels

There are six types of common transport channels: BCH, FACH, PCH, RACH, CPCH and DSCH.

BCH - Broadcast Channel

BCH is a downlink transport channel used to broadcast system specific and cell specific information such as spreading and scrambling codes that are in use etc. The BCH is always transmitted over the entire cell. BCH has fixed transport format.

FACH - Forward Access Channel

FACH is a downlink transport channel that is shared among different users to carry shared data. The FACH is transmitted over the entire cell or over only a part of the cell.

PCH - Paging Channel

PCH is a downlink transport channel used to carry paging information for UE. The PCH is always transmitted over the entire cell.

RACH - Random Access Channel

RACH is an uplink transport channel that is shared among different users to carry shared data. The RACH is characterized by a collision risk and is transmitted using open loop power control.

CPCH - Common Packet Channel

CPCH is an uplink transport channel used to transmit shared data among different users

DSCH - Downlink Shared Channel

DSCH is a downlink transport channel shared by several UEs. The DSCH is associated with one or several downlink DCH.

3.3 Indicators

Indicators are the physical layer generated bits used for control operations such as collision detection indication on shared channels, channel assignment indication, paging indication. They have specific format and the meaning of that specific format is known to the receiving end. There is no need for higher layers to know about the format and meaning of indicator bits. The different indicators are Acquisition Indicator (AI), Access Preamble Indicator (API), Channel Assignment Indicator (CAI), Collision Detection Indicator (CDI), Page Indicator (PI) and Status Indicator (SI) Indicator bits are transmitted on physical channels called indicator channels (ICHs).

3.4 Physical channels

Data from BS to UE is transmitted on downlink (forward link) physical channels and from UE to BS is transmitted on uplink (reverse link) physical channels. In FDD, a downlink physical channel is defined by a specific carrier frequency, scrambling code, and channelisation code (spreading code). In FDD an uplink physical channel is defined by a specific carrier frequency, scrambling code, spreading code and relative phase (0 or $\pi/2$). In TDD both uplink and downlink channels are defined with start and stop interval in addition to that of FDD definition. Time duration is defined by start and stop instants, measured in integer multiples of chips. Some basic definitions in WCDMA are

Radio frame: A radio frame is a processing duration that consists of 15 slots. The length of a radio frame corresponds to 38400 chips.

Slot: A slot is a duration, which consists of fields containing bits The length of a slot corresponds to 2560 chips. Each slot is individually power controlled.

The physical layer offers data transport services to higher layers and receives services from higher layers. The access to these services is through the use of transport channels via the MAC layer. The physical layer is expected to perform following functions in order to provide the data transport service:

- Error detection on transport channels and indication thereof to higher layers.
- FEC encoding/decoding of transport channels
- Multiplexing of transport channels and demultiplexing of coded composite transport channels (CCTrCHs)
- Rate matching of coded transport channels to physical channels.
- Mapping of coded composite transport channels on physical channels.
- Power weighting and combining of physical channels.
- Modulation and spreading/demodulation and despreading of physical channels
- Frequency and time (chip, bit, slot, frame) synchronisation.
- RF processing.

In this thesis, as we are implementing only downlink physical channels a brief summary of uplink physical channels and complete details of all downlink physical channels is given in this and next section. Complete details of all uplink channels are given in [18] in detail.

Both uplink and downlink physical channels are classified into

- Dedicated uplink/downlink physical channels – dedicated to particular user for a session.
- Common uplink/downlink physical channels – shared among different users.

3.4.1 Uplink physical channels

There are two types of dedicated uplink physical channels, the uplink Dedicated Physical Data Channel (uplink DPDCH) and the uplink Dedicated Physical Control Channel (uplink DPCCH). There are two types of common uplink physical channels, the Physical Random Access Channel (PRACH) and the Physical Common Packet Channel (PCPCH).

The uplink DPDCH is used to transmit voice and data from higher layers and uplink DPCCH is used to transmit physical layer control bits such as pilot bits, transmit power control (TPC) bits, Transport Format Combination Indicator bits (TFCI) TFCI indicates the receiver about the transport channels that are mapped onto DPDCH DPDCH and DPCCH are I/Q multiplexed and transmitted for each radio frame. Frame duration of DPDCH and DPCCH is 10 ms duration divided into 15 slots each of 2560 chips. Number of bits in each slot depends upon the spreading factor used. SF varies from 256 to 4 for DPDCH and is fixed as 256 for DPCCH. The frame formats, number of bits for different spreading factors for each slot, pilot bit patterns are given in detail in [18].

PRACH is used to carry RACH transport channel data. Inorder to transmit data, a UE has to acquire channel first by using slotted ALOHA approach by transmitting a preamble. After acquiring channel, data transmission takes place. Each 20 ms duration frame is divided into 15 slots of 5120 chips duration. Each slot is called an access slot. An UE can begin acquiring the channel at start of any access slot by transmitting a preamble of length 4096 chips. As more than one user may try at the same time to acquire the channel, collisions may occur. Say, after some number of attempts one UE succeeds and acquires the channel. After acquiring the channel, data is transmitted for 10 ms or multiple of 10 ms duration. The details of frame formats, SF used is given in detail in [18].

PCPCH is used to transmit CPCH transport channel data. Transmission of CPCH is based on Digital Sense Multiple Access with Collision Detection. The structure of transmission consists of one or several access preambles each of length 4096 chips, followed by one collision detection part, followed by power control preamble part of 0 or 8 slots in length and followed by a message of 10 ms duration or multiple of 10ms duration. SF of control part is fixed as 256 while for data it will vary from 256 to 4. Frame format and all other details of PCPCH can be seen in [18].

3.4.2 Downlink physical channels

Different downlink physical channels are explained in detail in this section

3.4.2.1 Dedicated downlink physical channels

There is only one type of dedicated downlink physical channel, the downlink Dedicated Physical Channel (downlink DPCH). Dedicated data from higher layers is transmitted on

Dedicated Physical Data Channel (DPDCH) and control information generated at Layer 1 (pilot bits, TPC commands, TFCI) is transmitted on Dedicated Physical Control Channel

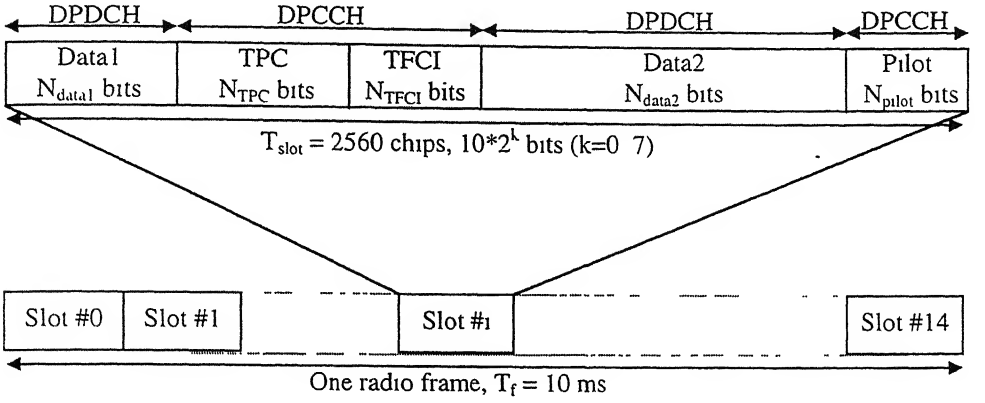


Figure 3.2: Frame format of downlink Dedicated Physical Channel

(DPCCH). DPDCH and DPCCH are time multiplexed and transmitted on downlink DPCH. Data transmitted on DPDCH is mapped onto two parts shown as Data1 and Data2 as shown in Figure 3.2.

Table 3.1: DPDCH and DPCCH fields

Slot Format Number	Channel Bit Rate (kbps)	Channel Symbol Rate(ksps)	SF	Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
					N_{Data1}	N_{Data2}	N_{TPC}	N_{TFCI}	N_{Pilot}
0	15	7.5	512	10	0	4	2	0	4
1	30	15	256	20	2	12	2	0	4
2	60	30	128	40	6	28	2	0	4
3	120	60	64	80	12	48	4	8	8
4	240	120	32	160	28	112	4	8	8
5	480	240	16	320	56	232	8	8	16
6	960	480	8	640	120	488	8	8	16
7	1920	960	4	1280	248	1000	8	8	16

Figure 3.2 shows the frame structure of the downlink DPCH. Each frame of length 10 ms is split into 15 slots each of 2560 chips length. The parameter k in Figure 3.2 determines the number of bits transmitted in each slot and is related to the spreading factor SF as $SF = 512/2^k$. The spreading factor ranges from 512 to 4.

The number of bits of the different downlink DPCH fields (N_{Pilot}, N_{TPC}, N_{TFCI}, N_{data1} and N_{data2}) is given in Table 3.1. The slot format to be used is configured by higher layers and can also be reconfigured by higher layers. The pilot bit patterns, relationship between the TPC symbol and the transmitter power control command are described in [18]. All dedicated downlink transport channels are mapped onto downlink DPCH.

3.4.2.2 Common downlink physical channels

3.4.2.2.1 Common Pilot Channel (CPICH)

The CPICH is a fixed rate (30 kbps) downlink physical channel used to carry a pre-defined bit sequence for initial synchronization. Figure 3.3 shows the frame format of the CPICH. The spreading used is fixed to 256.

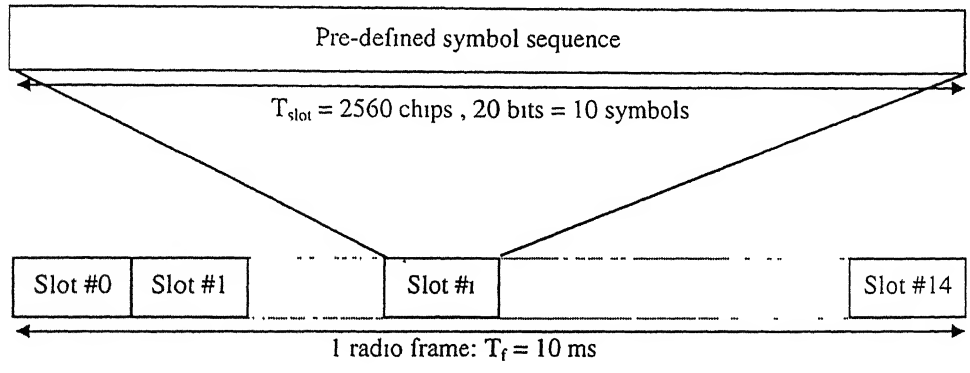


Figure 3.3: Frame format of Common Pilot Channel

3.4.2.2.2 Primary Common Control Physical Channel (PCCPCH)

The Primary CCPCH is a fixed rate (30 kbps) downlink physical channel used to carry

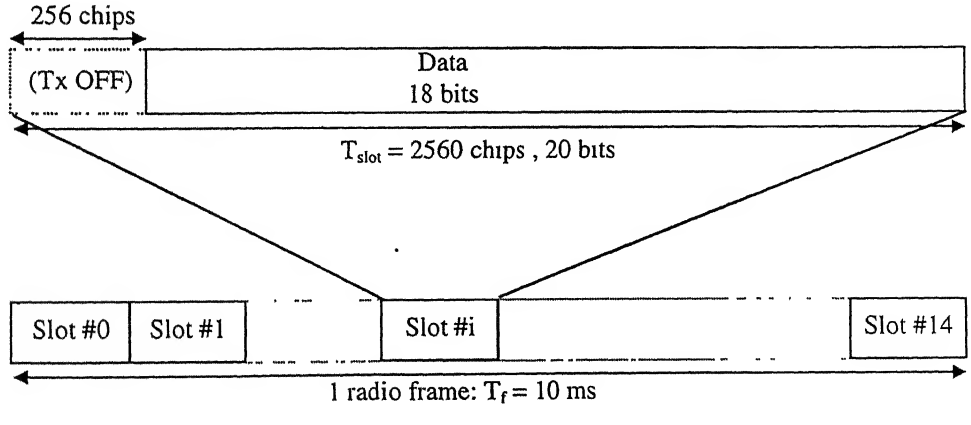


Figure 3.4: Frame format of Primary Common Control Physical Channel

the BCH transport channel data. Data on BCH informs the UE about the current spreading and scrambling codes used in BS, the power levels to be used. Data on BCH is needed for UE before starting a session. Spreading factor used for PCCPCH is fixed as 256. Figure 3.4 shows the frame structure of the Primary CCPCH. Each frame of duration 10 ms is divided into 15 slots of 2560 chips each. PCCPCH is not transmitted during the first 256 chips of each slot. Synchronisation channel (SCH) is transmitted during this period as explained in section 3.4.1.2.4.

3.4.2.2.3 Secondary Common Control Physical Channel (SCCPCH)

The Secondary CCPCH is used to carry the FACH and PCH transport channel data. FACH and PCH can be mapped onto the same or onto different SCCPCHs.

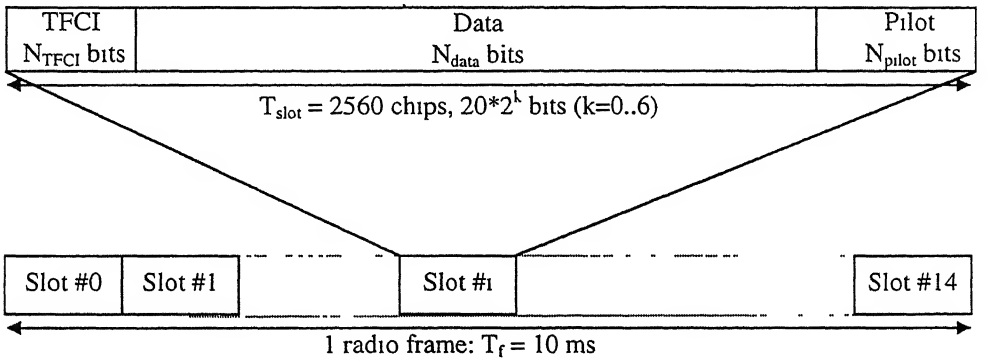


Figure 3.5: Frame format of Secondary Common Control Physical Channel

The frame structure of the SCCPCH is shown in Figure 3.5. Each frame of 10 ms duration is divided into 15 slots of 2560 chips each. The parameter k in Figure 3.5 determines the total number of bits per SCCPCH slot. It is related to the spreading factor as $SF = 256/2^k$. The SF of SCCPCH varies from 256 to 4. The exact number of bits of different fields is given in Table 3.2.The pilot bit patterns are given in [18].

The difference between PCCPCH and SCCPCH is that PCCPCH has a predefined transport format while transport format of SCCPCH can be changed and conveyed to the receiver by using TFCI field. Another difference is that PCCPCH should be transmitted in the completed cell while an SCCPCH carrying only FACHs can be transmitted in some part of cell by using beam forming antennas.

Table 3.2: Secondary CCPCH fields

Slot Format number	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
0	30	15	256	300	20	12	8	0
1	60	30	128	600	40	32	8	0
2	120	60	64	1200	80	64	8	8
3	240	120	32	2400	160	144	8	8
4	480	240	16	4800	320	296	16	8
5	960	480	8	9600	640	616	16	8
6	1920	960	4	19200	1280	1256	16	8

3.4.2.2.4 Synchronisation Channel (SCH)

The Synchronisation Channel (SCH) is a downlink channel used for UE synchronization cell search. The SCH consists of two sub channels, the Primary and Secondary SCH. The 10 ms radio frames of SCH is divided into 15 slots, each of length 2560 chips. SCH data is transmitted only during first 256 chips of each slot. During remaining part of each slot PCCPCH is transmitted as explained in section 3.4.2.2.2.

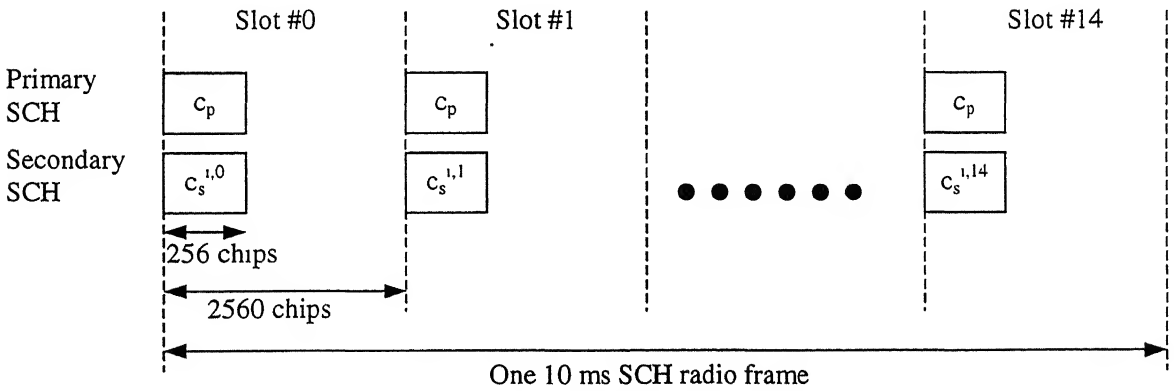


Figure 3.6: Frame format of Synchronisation Channel

Figure 3.6 illustrates the structure of the SCH radio frame. Two SCHs, primary SCH and secondary SCH, are transmitted in parallel in every slot during first 256 chips. The Primary SCH consists of a modulated code of length 256 chips called as the Primary Synchronisation Code (PSC) denoted as c_p in Figure 3.6. PSC is transmitted once for every slot. The PSC is the same for every cell in the system. The Secondary SCH consists

of repeatedly transmitting a length 15 sequence of modulated codes of length 256 chips called as Secondary Synchronisation Codes (SSC). The SSC is denoted as $c_s^{i,k}$ in Figure 3 6, where i = 0, 1, ..., 63 is the number of the scrambling code group, and k = 0, 1, ..., 14 is the slot number. Each SSC is chosen from a set of 16 different codes of length 256. This sequence on the Secondary SCH indicates which of the code groups the cell's downlink scrambling code belongs to. The PSC and SSCs are given in [19].

3.4.2.2.5 Physical Downlink Shared Channel (PDSCH)

The Physical Downlink Shared Channel (PDSCH) is shared channel and is used to carry DSCH transport channel data. A PDSCH is allocated on a radio frame basis to a single UE. The frame structure of the PDSCH is shown in Figure 3.7.

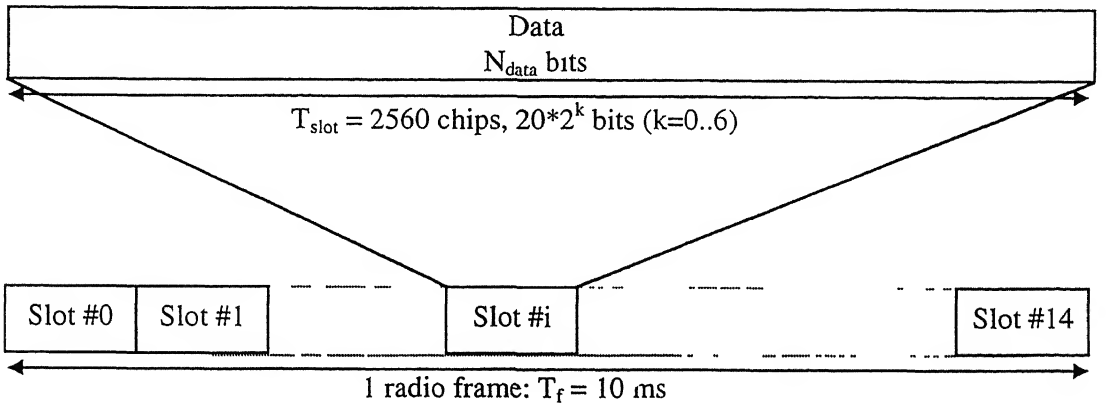


Figure 3.7: Frame format of physical downlink shared channel

PDSCH do not carry layer 1 control information. All layer 1 control information of PDSCH is transmitted on the DPDCH part of the associated DPCH. The UE will be informed that there is data to be received on the DSCH either using the TFCI field of the associated DPCH or by higher layer signalling that is carried on the associated DPCH. In TFCI based signalling the TFCI informs the UE of the instantaneous transport format parameters related to the PDSCH as well as the channelisation code of the PDSCH. In the other case, the information is given by higher layer signalling.

The channel bit rates and symbol rates for PDSCH are given in Table 3.3. For PDSCH spreading factor varies from 256 to 4.

Table 3.3: PDSCH fields

Slot format number	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
0	30	15	256	300	20	20
1	60	30	128	600	40	40
2	120	60	64	1200	80	80
3	240	120	32	2400	160	160
4	480	240	16	4800	320	320
5	960	480	8	9600	640	640
6	1920	960	4	19200	1280	1280

3.4.2.2.6 Acquisition Indicator Channel (AICH)

The Acquisition Indicator channel (AICH) is indicator channel (physical channel) used to carry Acquisition Indicators (AI). Acquisition Indicator AI_s corresponds to signature s on the uplink RACH. The SF used is fixed as 256. Figure 3.8 illustrates the frame structure of the AICH.

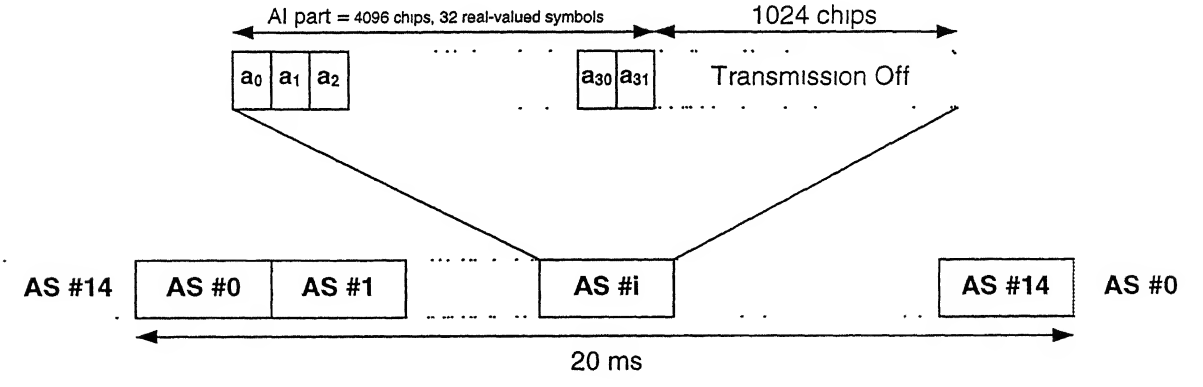


Figure 3.8: Frame format of Acquisition Indicator Channel

Each frame of duration 20 ms is divided into 15 slots called as access slots. Each access slot is of length 5120 chips. Each access slot is divided into two parts, an Acquisition Indicator (AI) part consisting of 32 real-valued symbols $a_0, \ldots, a_{31}$ and a part of duration 1024 chips with no transmission. 32 AI bits are transmitted in first pat of slot with 16 bits on I channel multiplexed with 16 bits on Q channel.

The real-valued symbols $a_0, a_1, \ldots, a_{31}$ in Figure 3.8 are given by

$$a_l = \sum_{s=0}^{15} AI_s b_{s,l}$$

where AI_s, taking the values +1, -1, and 0, is the acquisition indicator corresponding to signature s and the sequence $b_{s,0}, \ldots, b_{s,31}$ is as given in Table 3 4.

Table 3.4: AICH signature patterns

s	$b_{s,0}, b_{s,1} \ldots, b_{s,31}$																															
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1
2	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1
3	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1
4	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1
5	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1
6	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1
7	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1
8	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
9	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
10	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
11	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1
12	1	1	1	1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1
13	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
14	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	1	1	1	1	-1	-1	-1	-1
15	1	1	-1	-1	-1	-1	1	1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1	-1	-1	1	1	-1	-1	-1	-1	1	1

3.4.2.2.7 CPCH Access Preamble Acquisition Indicator Channel (AP-AICH)

The Access Preamble Acquisition Indicator channel (AP-AICH) is indicator channel (physical channel) used to carry AP acquisition indicators (API) of CPCH. AP acquisition indicator API_s corresponds to AP signature s transmitted by UE. Figure 3.9 illustrates the frame format of AP-AICH.

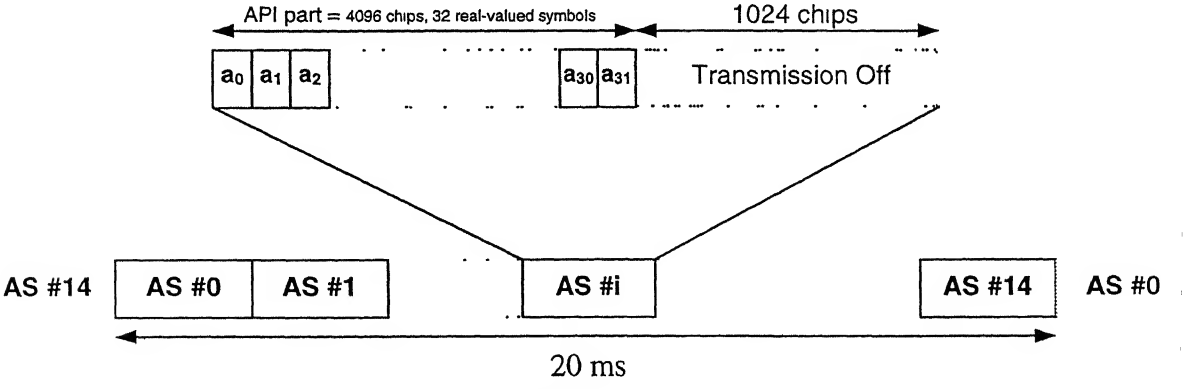


Figure 3.9: Frame format of Access Preamble Acquisition Indicator Channel

Each frame of 20 ms duration is divided into 15 slots of 5120 chips each. Each slot is divided into two parts with first part of 4096 chips length where the AP acquisition indicator (API) is transmitted, followed by a part of duration 1024 chips with no

transmission. 32 API bits are transmitted in first pat of slot with 16 bits on I channel multiplexed with 16 bits on Q channel. The SF to be used is fixed to 256.

The real-valued symbols $a_0, a_1, \ldots, a_{31}$ in Figure 3.9 are given by

$$a_i = \sum_{s=0}^{15} API_s \times b_{s,i}$$

where API_s, taking the values +1, -1, and 0, is the AP acquisition indicator corresponding to Access Preamble signature s transmitted by UE and the sequence $b_{s,0}, \ldots, b_{s,31}$ is as given in Table 3.4.

3.4.2.2.8 CPCH Collision Detection/Channel Assignment Indicator Channel (CD/CA-ICH)

The Collision Detection/Channel Assignment Indicator channel (CD/CA-ICH) is indicator channel used to carry Collision Detector Indicator (CDI) if the channel assignment is not active, or Collision Detection Indicator/Channel Assignment Indicator (CDI/CAI) at the same time if the channel assignment is active. The structure of CD/CA-ICH is shown in Figure 3.10.

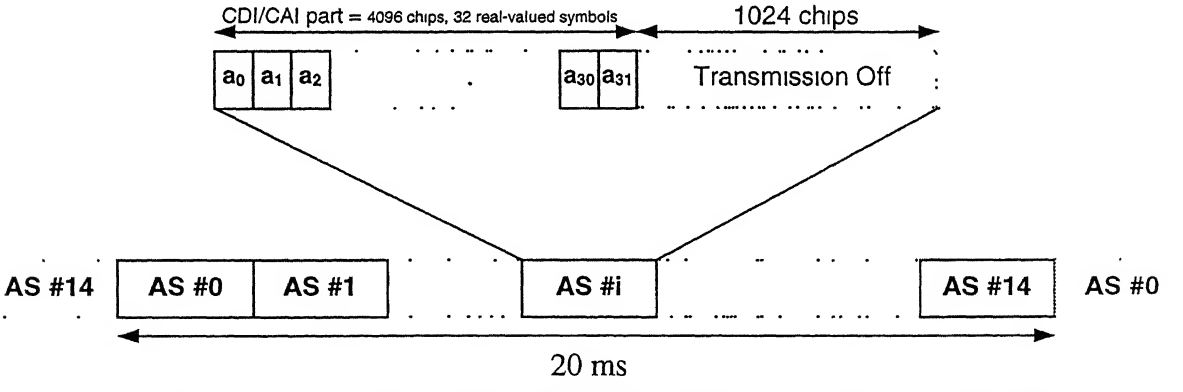


Figure 3.10: Frame format of Collision detection/Channel Assignment Indicator ch.

Each frame of 20 ms duration is divided into 15 slots of 5120 chips each. Each slot is divided into two parts with first part of 4096 chips length where the CDI/CAI is transmitted followed by a part of duration 1024 chips with no transmission. The part of the slot with no transmission is reserved for possible future use by other physical channels. 32 indicator bits are transmitted in first part of slot with 16 indicator bits on I channel multiplexed with 16 indicator bits on Q channel. The SF used is fixed as 256.

In case CA is not active, the real-valued symbols a_0, a_1, ..., a_{31} in Figure 3.10 are given by

$$a_i = \sum_{s=0}^{15} CDI_s \times b_{s,i}$$

where CDI_s, taking the values +1 and 0, is the CD indicator corresponding to CD preamble signature s transmitted by UE and the sequence $b_{s,0}$, ..., $b_{s,31}$ is as given in Table 3.4.

In case CA is active, the real-valued symbols a_0, a_1,..., a_{31} in Figure 3.10 are given by

$$a_i = \sum_{i=0}^{15} CDI_i \times b_{s_i,i} + \sum_{k=0}^{15} CAI_k \times b_{s_k,i}$$

where the subscript s_i, s_k depend on the indexes i, k according to Table 21 in [18]. The sequence $b_{s,0}$, ..., $b_{s,31}$ is given in Table 3.4. CDI_i takes the values +1/0 or -1/0, is the CD indicator corresponding to the CD preamble i transmitted by the UE, and CAI_k takes the values +1/0 or -1/0, is the CA indicator corresponding to the assigned channel index k as given in Table 21 in [18].

3.4.2.2.9 Paging Indicator Channel (PICH)

The Paging Indicator Channel (PICH) is used to carry the Paging Indicators (PI). Figure 3.11 illustrates the frame structure of the PICH. One PICH radio frame of length 10 ms consists of 300 bits (b_0, b_1, ..., b_{299}). Of these, 288 bits (b_0, b_1, ..., b_{287}) are used to carry Paging Indicators and the remaining 12 bits are not formally part of the PICH and shall not be transmitted. The SF used is fixed as 256.

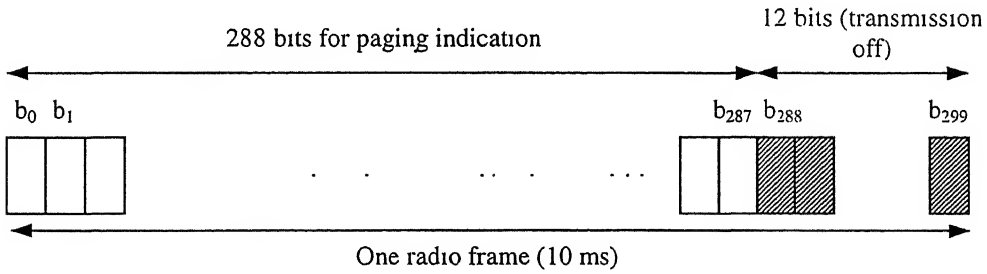


Figure 3.11: Frame format of Paging Indicator Channel

N Paging Indicators {PI_0, ..., PI_{N-1}} are transmitted in each PICH frame, where N=18, 36, 72, or 144. The PI calculated by higher layers for a certain UE is mapped to the paging indicator PI. If a Paging Indicator in a certain frame is set to "1" it is an

indication that UEs associated with this Paging Indicator should read the corresponding frame of the associated SCCPCH.

3.4.2.2.10 CPCH Status Indicator Channel (CSICH)

The CPCH Status Indicator Channel (CSICH) is an indicator channel used to carry uplink CPCH status information. Figure 3.12 illustrates the frame structure of the CSICH.

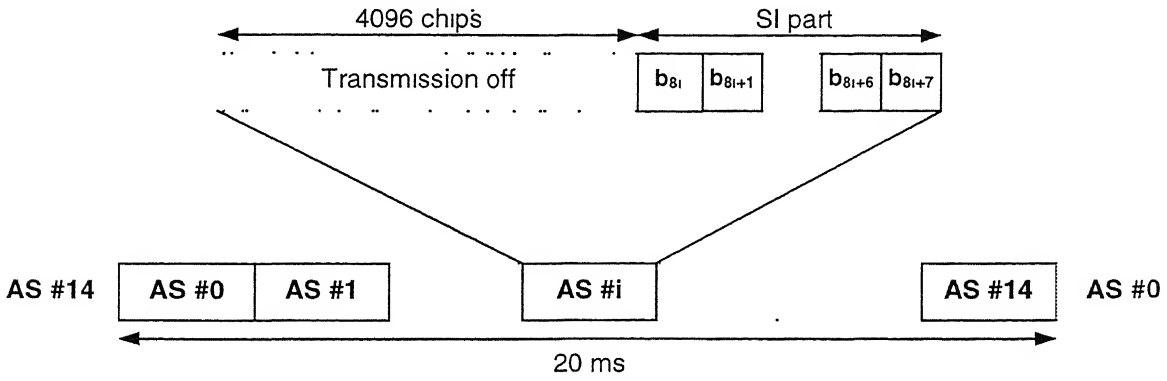


Figure 3.12: Frame format of Common packet channel Status Indicator Channel

Each frame is of 20 ms duration and is divided into 15 slots of 5120 chips each Each slot is divided into two parts with first part of 4096 chips length with no transmission followed by a part of duration 1024 chips where 8 status indicator bits are transmitted. 8 indicator bits are transmitted in second part of slot with 4 indicator bits on I channel multiplexed with 4 indicator bits on Q channel The SF used is fixed as 256.

N Status Indicators $\{SI_0, \ldots, SI_{N-1}\}$ are transmitted in each CSICH frame. The mapping from $\{SI_0, \ldots, SI_{N-1}\}$ to the CSICH bits $\{b_0, \ldots, b_{119}\}$ is according to Table 23 in [18].

3.5 Mapping of transport channels onto physical channels

Figure 3.13 summarizes the mapping of transport channels onto physical channels.

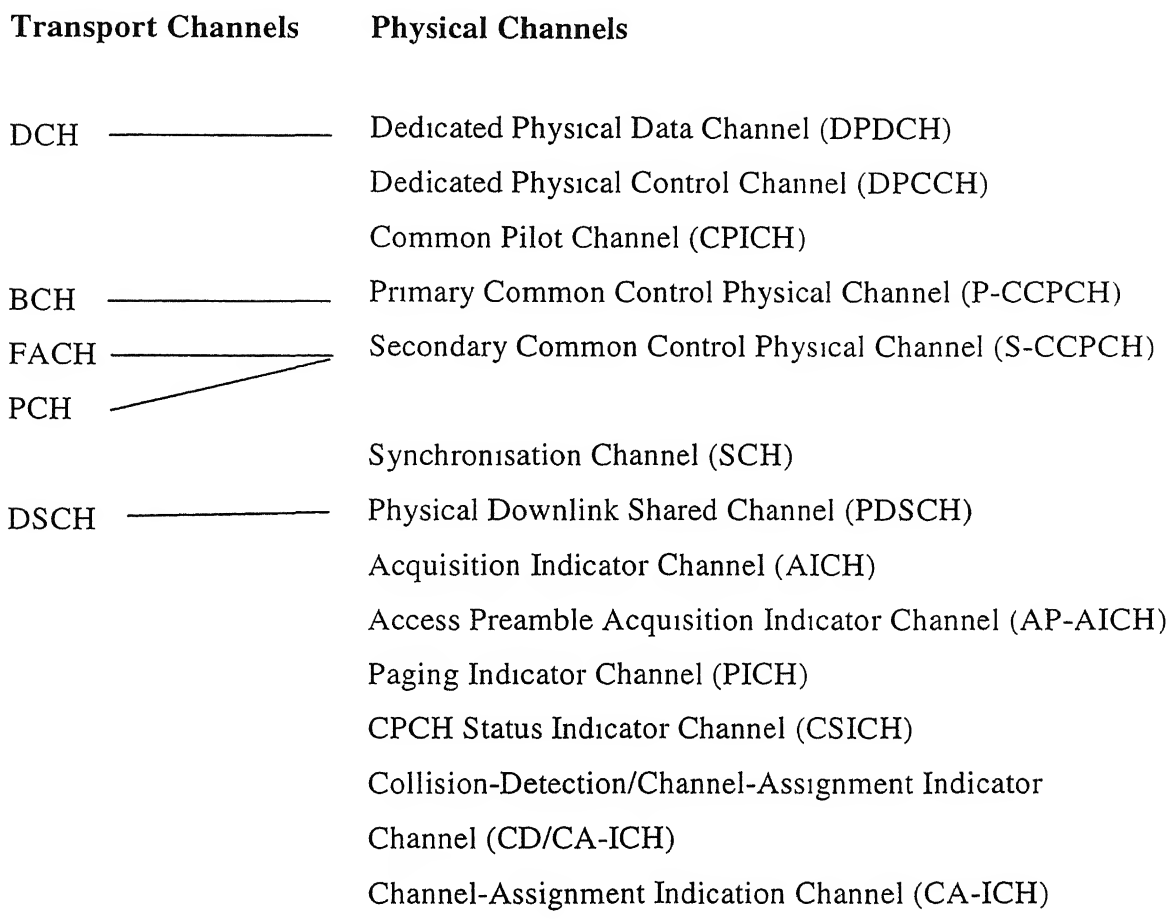


Figure 3.13: Transport-channel to physical-channel mapping of downlink channels

The DCHs are coded and multiplexed as described in next Chapter, given in more detail in [20], and the resulting data stream is mapped sequentially (first-in-first-mapped) directly to the physical channel(s). The mapping of BCH and FACH/PCH is equally straightforward, where the data stream after coding and interleaving is mapped sequentially to the Primary and Secondary CCPCH respectively.

Chapter 4

WCDMA physical layer – Description of physical layer operations (FDD)

This chapter continues the discussion on physical layer of WCDMA (FDD). It explains the physical layer operations such as CRC coding, channel coding, rate matching, interleaving, spreading, scrambling and modulation.

4.1 Operations to be performed on transport channels in mapping to physical channels

Data stream from/to MAC and higher layers is encoded/decoded to offer transport services over the radio transmission link. Data arrives to the physical layer from MAC in the form of transport blocks once every transmission time interval (TTI) The number of blocks in each TTI depends upon type of channel and is given later in this chapter. The size of each transport block is fixed as 336 bits or 576 bits depending on the type of data channel. The transmission time interval can be any one of 10 ms or 20 ms or 40 ms or 80 ms depending upon the type of the channel.

Following operations are to be performed (explained in next section) on each transport block of all downlink transport channels in mapping them onto physical channels:

- CRC coding.
- Transport block concatenation and code block segmentation
- Channel coding.
- Rate matching.
- Insertion of discontinuous transmission (DTX) indication.
- Interleaving.
- Radio frame segmentation.
- Multiplexing of transport channels into coded composite transport channel.
- Physical channel segmentation.
- mapping to physical channels.

These steps for downlink are shown in Figure 4.1 and explained in detail in next section.

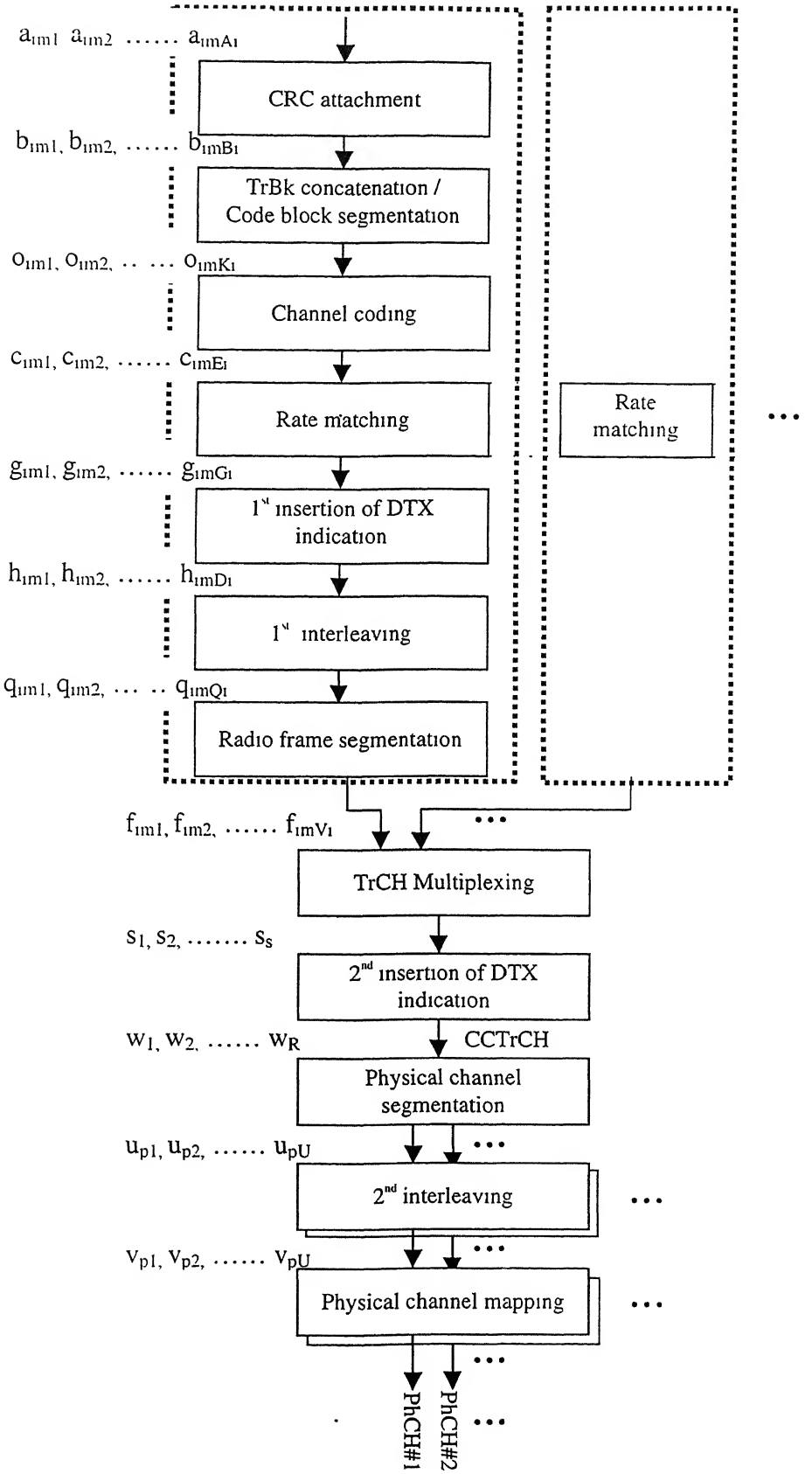


Figure 4.1: Transport channel multiplexing structure for downlink

Data on all the transport channels in a TTI are serially multiplexed called as TrCH multiplexing and the resultant data stream is called Coded Composite Transport Channel (CCTrCH).

4.1.1 Error detection

Error detection is provided on bits of transport blocks by using Cyclic Redundancy Check (CRC) code. The number of CRC bits can be any one of 24, 16, 12, 8 or 0. Number of CRC bits to be used for each TrCH is indicated by higher layers.

4.1.1.1 CRC Calculation

All the bits of each transport block are used to calculate the CRC bits. Any one of the following cyclic generator polynomials are used to generate the CRC bits:

- $g_{CRC24}(D) = D^{24} + D^{23} + D^6 + D^5 + D + 1.$
- $g_{CRC16}(D) = D^{16} + D^{12} + D^5 + 1.$
- $g_{CRC12}(D) = D^{12} + D^{11} + D^3 + D^2 + D + 1.$
- $g_{CRC8}(D) = D^8 + D^7 + D^4 + D^3 + D + 1.$

4.1.2 Transport block concatenation and code block segmentation

All transport blocks in a TTI are serially concatenated.

As there is a maximum limit on the size of block input to channel coder, if the number of bits in concatenated block is larger than a certain value, code block segmentation is to be done after the concatenation of the transport blocks. The maximum size of code block depends on type of channel-coding used. All code blocks after code block segmentation are of equal size. If the number of bits input to the segmentation is not a multiple of number of code blocks, filler bits are added to the beginning of the first code block. The filler bits are always set to 0 and are transmitted.

The maximum code block sizes are:

- Convolutional coding : 504
- Turbo coding : 5114
- No coding : unlimited.

4.1.3 Channel coding

Channel coding is performed on code blocks after transport block concatenation and code block segmentation.

Any one of the following channel coding schemes can be used depending on the quality of service needed for each transport channel. For required bit error rates around 10^{-6} turbo coding is used and for bit error rates around 10^{-3} convolutional coding is used.

- Convolutional coding (rate 1/2 and 1/3).
- Turbo coding.

Channel coding scheme to be used for some channels is given in Table 4.1. The relation between number of input bits (I) and number of output bits (O) for different channel coding schemes are as follows:

- Convolutional coding - rate 1/2: O = 2*I + 2*8, rate 1/3: O= 3*I+ 3*8.
- Turbo coding O= 3* I+ 12.

Table 4.1: Type of channel coding for different type of channels

Type of TrCH	Coding scheme	Coding rate
BCH,PCH	Convolutional coding	1/2
CPCH, DCH, DSCH, FACH	Convolutional coding	1/3, 1/2
	Turbo coding	1/3
	No coding	

4.1.3.1 Convolutional coding

The constraint length of convolutional coder used is 9. Both rate 1/3 and rate 1/2 are used. The structure of the convolutional coder is shown in Figure 4.2. The initial value of all the shift registers of the coder is set to 0 before starting to encode the input bits. 8 tail bits with value 0 are added to the end of the code block before encoding. Tail bits are appended to clear the convolutional coder after encoding each block. It is basically initializing the coder. By clearing convolutional coder after encoding each block, the dependency of the output bits of one block on its previous input block bits is removed.

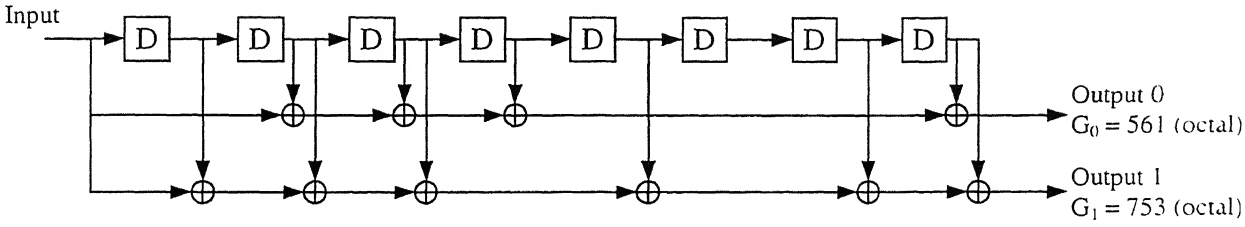
4.1.3.2 Turbo coding

The Turbo coder used is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one Turbo code internal interleaver. Rate of Turbo coder used is 1/3. The structure of Turbo coder is as shown in Figure 4.3.

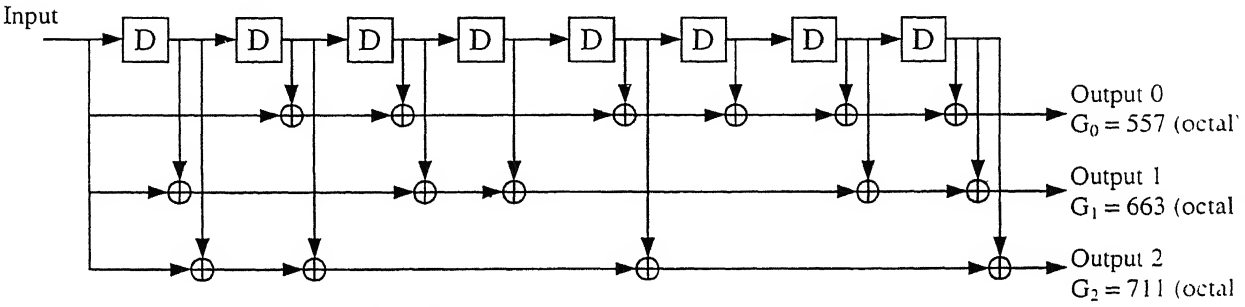
The transfer function of the 8-state constituent code for PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right], \quad \text{where}$$

$$g_0(D) = 1 + D^2 + D^3,\ g_1(D) = 1 + D + D^3$$



(a) Rate 1/2 convolutional coder



(b) Rate 1/3 convolutional coder

Figure 4.2: Structure of rate 1/2 and rate 1/3 convolutional coders

Let $x_1, x_2, \ldots, x_K$ are the input bits to the Turbo coder (bits input to first 8-state constituent encoder), $x'_1, x'_2, \ldots, x'_K$. are the bits output from interleaver and these bits are input to second 8-state constituent encoder (interleaved input bits), $z_1, z_2, \ldots, z_K$ and $z'_1, z'_2, \ldots, z'_K$ are the output bits from first and second 8-state constituent encoders respectively and K is the number of bits, the output sequence of bits from the Turbo coder are $x_1, z_1, z'_1, x_2, z_2, z'_2, \ldots, x_K, z_K, z'_K$. The initial values of the shift registers of both 8-state constituent encoders are set to zeros.

After all input information bits are encoded, output bits of encoders are fed back (shown in Figure 4.3 with dotted lines) for termination. Three output bits of first encoder are used to terminate the first constituent encoder (switch before first encoder in Figure 4.3 in lower position) with the second constituent encoder disabled. Three output bits of second encoder are used to terminate the second constituent encoder (switch before second encoder in Figure 4.3 in lower position) with the first constituent encoder

disabled. Then the transmitted tail bits are x_{K+1}, z_{K+1}, x_{K+2}, z_{K+2}, x_{K+3}, z_{K+3}, x'_{K+1}, z'_{K+1}, x'_{K+2}, z'_{K+2}, x'_{K+3}, z'_{K+3}.

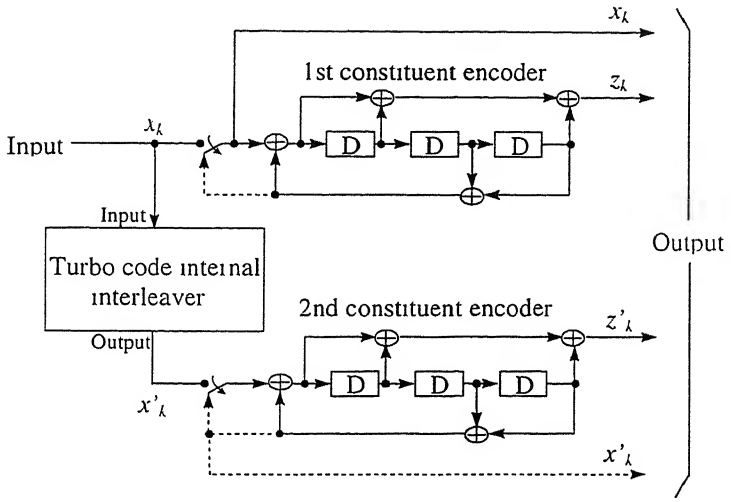


Figure 4.3: Structure of Turbo coder

The Turbo-coder internal interleaver consists of rectangular matrix to hold input bits. Intra-row and inter-row permutations are performed on bits of rectangular matrix. The output sequence is obtained by reading the bits from rectangular matrix by removing bits that are not present in input. Complete details of internal interleaver are given in detail in [20].

After channel coding (Turbo coding or convolutional coding) of each code block, the encoded blocks are serially concatenated so that the block with lowest index is outputted first from the channel coding block, otherwise the encoded block is outputted from channel coding block as it is. If no code blocks are input to the channel coding, no bits are output from the channel-coding block.

4.1.4 1st interleaving

The 1st interleaving is a block interleaver with inter-column permutations. The input bit sequence to the 1st interleaver is assumed and guaranteed to be an integer multiple of TTI. The 1st interleaving is done as follows:

1. Numbers of columns C1 are selected from Table 4.2 depending on TTI.
2. Number rows R1 are determined by $R1 = X_i / C1$, (X_i is the number of input bits)
3. The input bit sequence was written into a $R1 \times C1$ rectangular matrix row by row.

4. Inter-column permutation is done on rectangular matrix of bits based on the pattern of Table 4.2.
5. Output bit sequence was obtained by reading column by column from the inter-column permuted rectangular matrix of bits.

Table 4.2: Inter-column permutation patterns for 1st interleaving

TTI (ms)	Number of columns C1	Inter-column permutation patterns <P1(0),P2(0) ..., P1(C1-1)>
10	1	<0>
20	2	<0,1>
40	4	<0,2,1,3>
80	8	<0,4,2,6,1,5,3,7>

4.1.5 Radio frame segmentation

When the transmission time interval is longer than 10 ms, the input bit sequence is segmented and mapped onto consecutive radio frames. The input bit sequence length to radio frame segmentation is guaranteed to be an integer multiple of number of radio frames.

4.1.6 Rate matching

The numbers of bits on transport channels vary between different transmission time intervals. This variable rate data is to be transmitted on the final physical channel with fixed number of slots, by puncturing or repeating the bits, called as Rate Matching. Higher layers assign a rate-matching attribute for each TrCH and is used to determine the number of bits that can be punctured or repeated. If no bits are input to the rate matching on all TrCHs within a CCTrCH, no bits are output onto CCTrCH

Following notations are used in our subsequent discussions.

N_i^{TTI} : Number of bits in a TTI on TrCH i.

ΔN_i^{TTI} : Number of bits to be repeated (for positive value) or punctured (for negative value) in each transmission time interval on TrCH i.

RM_i : Rate Matching attribute for TrCH i.

N_{data} : Total number of bits available for the CCTrCH in a radio frame

I : Number of TrCHs in the CCTrCH.

$Z_{i,J}$: Intermediate calculation variable.

F_i : Number of radio frames in a TTI of TrCH i.

F_{max} : Maximum number of radio frames in a TTI

P : Number of physical channels on CCTrCH.

e_{ini}, e_{plus} e_{minus} are the Initial value, increment value and decrement value of variable e in the rate matching algorithm given in 4.1 6.3.

4.1.6.1 Determination of rate matching parameters in downlink

N_{data} depends on the channelisation code(s) assigned by the higher layers N_{data} is the number of bits available to the .CCTrCH in one radio frame and defined as $N_{data}=P\times15\times(N_{data1}+N_{data2})$, where N_{data1} and N_{data2} are defined in section 3 4 1.1and P is the number of physical channels used.

Following intermediate calculations are to be done for each TrCH in the CCTrCH in order to determine the bits that are to be rate matched.

Set $Z_{0} = 0$

$$Z_i = \left\lfloor \frac{\left(\left(\sum_{m=1}^{I} RM_m \times N_m \right) \times N_{data} \right)}{\sum_{m=1}^{I} RM_m \times N_m} \right\rfloor \qquad \text{for all } i = 1 \ldots I$$

$$\Delta N_i = Z_i - Z_{i-1} - N_i \qquad \text{for all } i = 1 \ldots I$$

if $\Delta N_i = 0$, no rate matching is to be done for TrCH i.

if $\Delta N_i \neq 0$, the parameters given next in this section are used as inputs for rate matching algorithm of 4.1.6.3.

For rate matching of uncoded and convolutionally encoded transport channels, following parameters are used as input for the rate-matching algorithm:

$a = 2$

$X_i = N_i^{TTI}$

$e_{ini} = 1$

$e_{plus} = a*N_i^{TTI}$

$e_{minus} = a*|\Delta N_i|$

If $\Delta N_i < 0$ puncturing is to be done, otherwise repetition is done. ΔN_i^{TTI} can be found by counting repetitions or puncturing when the rate-matching algorithm is run It is given by the following expression

$$N_i^{TTI} = \left| \frac{|\Delta N_i| \times X_i}{N_i^{TTI}} \right| \times \mathrm{sgn}(\Delta N_i)$$

For rate matching of Turbo encoded TrCHs if repetition is to be performed i.e. for $\Delta N_i > 0$, the parameters calculated for uncoded and convolutionally TrCHs are used.

If puncturing is to be performed, the parameters below are to be used:

Index b is used to indicate systematic (b=1), 1st parity (b=2), and 2nd parity bit (b=3).

The bits indicated by b=1 are not punctured.

a=2 for b=2

a=1 for b=3

$$N_i^b = \begin{cases} \lfloor \Delta N_i / 2 \rfloor, & \text{for } b = 2 \\ \lceil \Delta N_i / 2 \rceil, & \text{for } b = 3 \end{cases}$$

Next following parameters are used as input for rate matching algorithm

$$X_i = N_i^{TTI} / 3$$

$$e_{ini} = N_i^{TTI}$$

$$e_{plus} = a * N_i^{TTI}$$

$$e_{minus} = a * |\Delta N_i^b|$$

The values of ΔN_i^{TTI} can be found by counting puncturing when the rate matching algorithm is run. It is also given by the following expression.

$$N_{i,l}^{TTI} = -\left\lfloor \frac{|\Delta N_i^2| \times X_i}{N_i^{TTI}} + 0.5 \right\rfloor - \left\lfloor \frac{|\Delta N_i^3| \times X_i}{N_i^{TTI}} \right\rfloor$$

In the equation above, the first term of the right hand side represents the amount of puncturing for b=2 and the second term represents the amount of puncturing for b=3.

4.1.6.2 Bit separation and collection

The systematic bits of turbo encoded TrCHs are not punctured. The bits output from Turbo coder are separated into three sequences as systematic bits, first parity bits and second parity bits. Second (first parity bits) and third (second parity bits) sequences can be punctured whereas the first sequence is passed without any puncturing. During rate matching bits to be punctured are marked so that they can be removed later. After marking the bits to be punctured, all three sequences are combined into a single sequence that is an inverse process of bit separation. After bit collection, bits marked as punctured are removed.

This bit separation function is not done for uncoded TrCHs, convolutionally encoded TrCHs, and for turbo encoded TrCHs with repetition. The bit separation and bit collection is illustrated with figures in [20].

4.1.6.3 Rate matching algorithm

By denoting the bits input to rate matching block as x_{i1}, x_{i2}, x_{i3} K x_{iX_i}, where i is the TrCH number and using parameters X_i, e_{ini}, e_{plus}, and e_{minus} as given in previous section, the rate matching algorithm is shown in Figure 4.4 and is given as follows:

if puncturing is to be performed

$e = e_{ini}$

m = 1 -- index of current bit

do while $m \leq X_i$

$e = e - e_{minus}$ -- update error

if $e \leq 0$ then -- check if bit number m should be punctured

set bit $x_{i,m}$ to δ where $\delta \notin \{0, 1\}$ so that the bit can be removed.

$e = e + e_{plus}$

end if

m = m + 1 -- go to next bit

end do

else -- repetition to be done

$e = e_{ini}$

m = 1 -- index of current bit

do while $m \leq X_i$

$e = e - e_{minus}$ -- update error

do while $e \leq 0$ -- check if bit number m should be repeated

repeat bit $x_{i,m}$

$e = e + e_{plus}$ -- update error

end do

m = m + 1 -- go to next bit

end do

end if

A repeated bit is placed directly after the original one.

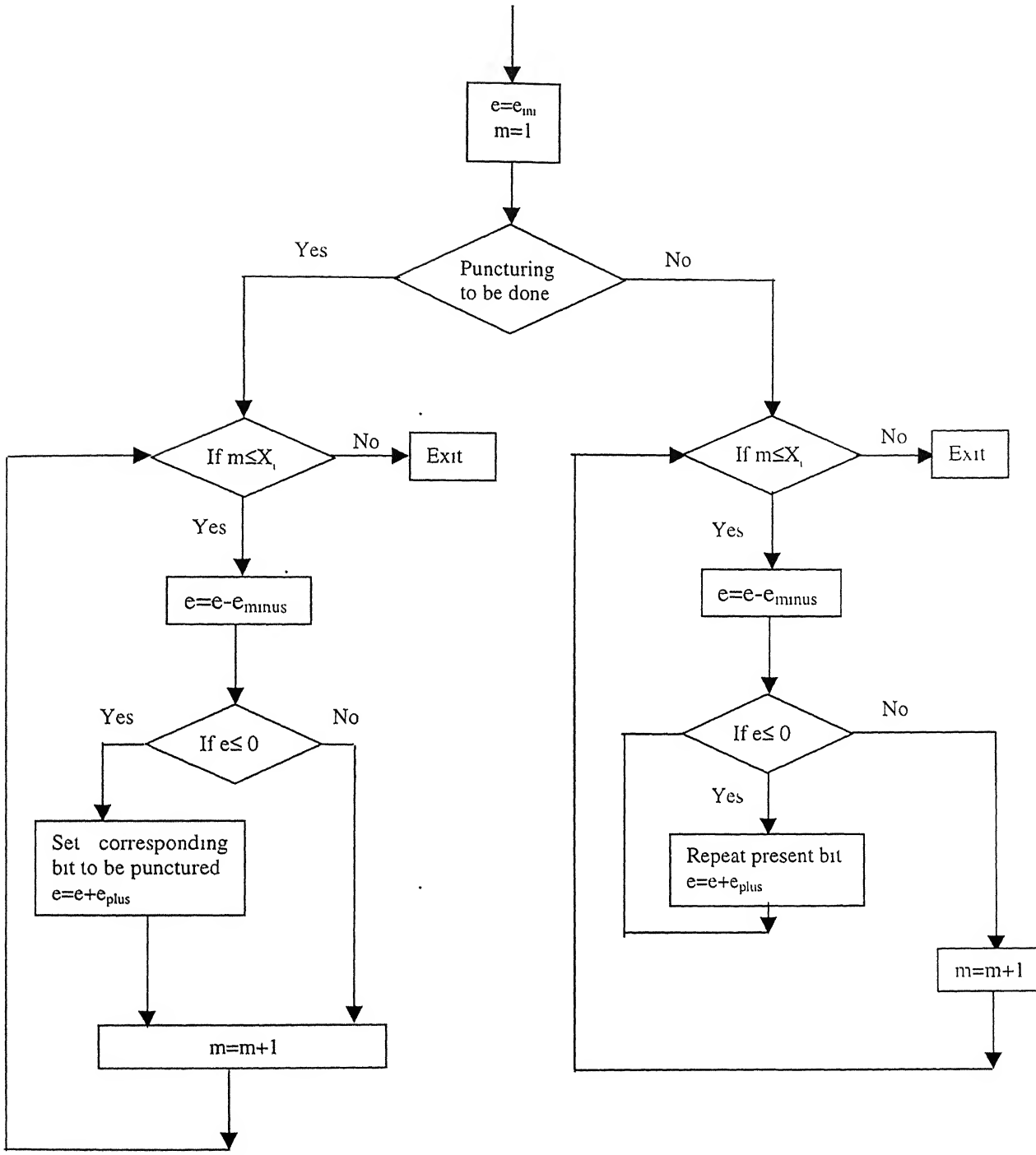


Figure 4.4: Rate matching algorithm

4.1.7 TrCH multiplexing

Every 10 ms, one radio frame from each TrCH is delivered to the TrCH multiplexing. Radio frames in each TTI from all transport channels are serially multiplexed and the resultant data stream is called as coded composite transport channel (CCTrCH).

4.1.8 Insertion of discontinuous transmission (DTX) indication bits

In the downlink, DTX is used to fill up the radio frame with bits. The insertion point of DTX indication bits depends on whether fixed or flexible positions of the TrCHs in the radio frame are used. It is up to the UTRAN to decide for each CCTrCH whether fixed or flexible positions are used during the connection. DTX indication bits indicate when the transmission is turned off.

DTX bits are inserted by spreading factor reduction, by additional puncturing or by higher layer scheduling. Insertion of DTX bits is given in detail in [20].

4.1.9 2nd interleaving

The 2nd interleaver is a block interleaver with inter-column permutations. Let U be the number of bits in one radio frame for one physical channel (PhCH).

Table 4.3: Inter-column permutation pattern for 2nd interleaving

Number of columns C2	Inter-column permutation pattern < P2(0), P2(1), ...,P2(29) >
30	0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1,11,21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17

The 2nd interleaving is done as follows

1. Number of columns C2 is set to 30.
2. Number of rows R2 is determined by finding minimum integer R2 such that $U \leq R2 \times C2$.
3. Input bits are written in a R2 × C2 rectangular matrix row by row.
4. Inter-column permutation on bits of rectangular matrix is done based on the pattern of Table 4.3.
5. Output bit sequence is obtained by reading the bits from the rectangular matrix column by column. Output bit sequence is read from rectangular matrix after deleting the bits that are not present in the input sequence.

4.2 Multiplexing of different transport channels into one CCTrCH and mapping of one CCTrCH onto physical channels

Following rules apply to the different transport channels that are part of the same CCTrCH:

- Only transport channels with the same set can be mapped onto the same CCTrCH.

- Different CCTrCHs cannot be mapped onto the same PhCH
- One CCTrCH can be mapped onto one or several PhCHs. All these physical channels should have the SF.
- Dedicated Transport channels and common transport channels cannot be multiplexed onto the same CCTrCH.
- For the common transport channels, only the FACH and PCH may belong to the same CCTrCH.

Thus, there are two types of CCTrCH:

- CCTrCH of dedicated type obtained by coding and multiplexing of one or several DCHs.
- CCTrCH of common type, obtained by coding and multiplexing of a common channels as RACH in the uplink, DSCH, BCH, or FACH/PCH for the downlink.

4.3 Spreading and modulation

4.3.1 Overview

After second interleaving, bits in a CCTrCH are mapped onto one or more physical channels. Spreading and scrambling is applied to bits on physical channels. The first operation is the spreading or channelisation, which transforms every data symbol into a number of chips by using an Orthogonal Variable Spreading Factor (OVSF) code thus increasing the bandwidth of the signal. The number of chips per data symbol is called the Spreading Factor (SF). The second operation is the scrambling operation where the spread bits are multiplied by a complex-valued scrambling code. The spread and scrambled bits are finally QPSK modulated after pulse shaping.

4.3.2 Spreading Codes

As number of bits on different channels varies, spreading codes of different length are needed that preserve the orthogonality between physical channels. The codes used are called Orthogonal Variable Spreading Factor (OVSF) codes. The codes of different length are orthogonal if allocated to different channels according to rules given in [21] and explained in brief in next chapter. The OVSF codes are defined using the code tree of Figure 4.5. In Figure 4.5, the codes are described as $C_{ch,SF,k}$, where SF is the spreading factor of the code and k is the code number, $0 \leq k \leq SF-1$. Each level in the code tree

defines channelisation codes of length SF. Generation of OVSF codes is given in detail in [21].

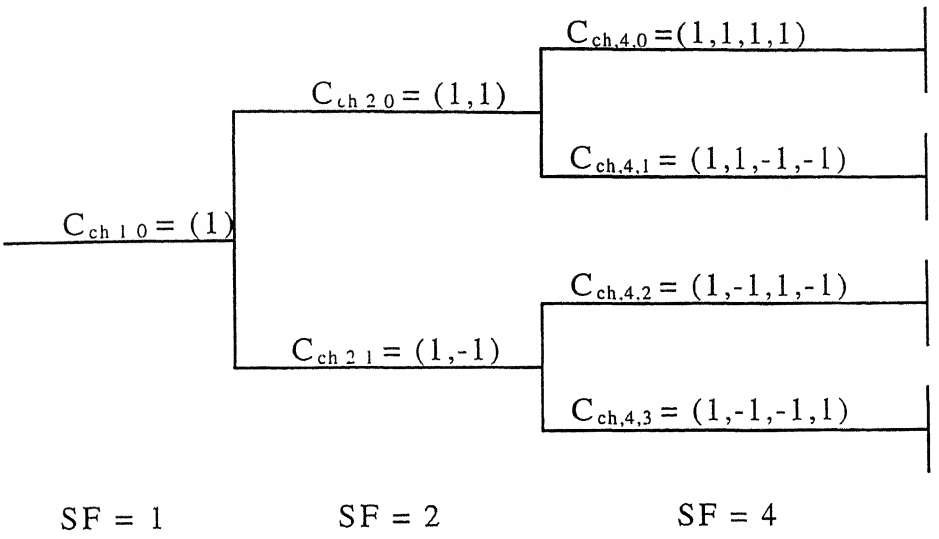


Figure 4.5: Code-tree for generation of OVSF codes

The spreading code for the Primary CPICH is fixed as $C_{ch,256,0}$ and the spreading code for the Primary CCPCH is fixed as $C_{ch,256,1}$.The spreading codes for all other physical channels are assigned by UTRAN.

4.3.3 Spreading

All downlink channels are spread by OVSF code. Figure 4.6 illustrates the spreading operation for all downlink physical channels except SCH.

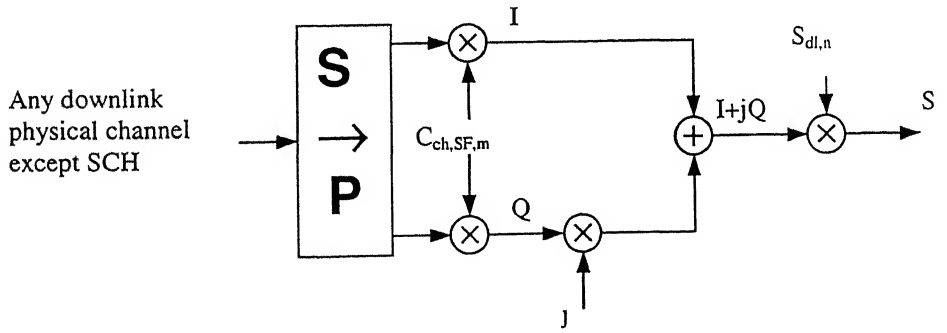


Figure 4.6: Spreading for all downlink physical channels except SCH

After physical channel mapping, each pair of two consecutive symbols is first serial-to-parallel converted and mapped to I and Q branches. The mapping is such that even and odd numbered symbols are mapped to I and Q branches respectively. The bits on both I and Q branches are then spread to the chip rate by using the same spreading

code. The sequences of real-valued chips on I and Q branches are then treated as a single complex-valued sequence of chips.

4.3.4 Scrambling

After the spreading chips on both I and Q channels are combined into a complex sequence. The complex valued sequence of chips are scrambled (complex chip-wise multiplication) by a complex-valued scrambling code $S_{dl,n}$.

Scrambling codes are constructed from two binary sequences each of length 18. A total of 2^{18}-1 = 262,143 scrambling codes can be generated. Among them only 8192 codes are used. These 8192 codes are divided into 512 sets each of primary scrambling code and 15 secondary scrambling codes. The set of primary scrambling codes is further divided into 64 scrambling code groups, each consisting of 8 scrambling codes.

Each cell is allocated one and only one primary scrambling code. The primary CCPCH and primary CPICH are always transmitted using the primary scrambling code. The other downlink physical channels can be transmitted with either the primary scrambling code or a secondary scrambling code from the set associated with the primary scrambling code of the cell.

The scrambling code sequences are constructed by combining two real sequences, x and y, into a complex sequence. Using two generator polynomials ($1+X^7+X^{18}$ and $1+X^5+X^7+ X^{10}+X^{18}$) generates the two real sequences of degree 18. The scrambling codes are repeated for every 10 ms radio frame.

Let x(i), y(i) and $z_n(i)$ denote the ith symbol of the sequence x, y, and z_n, respectively.

The m-sequences x and y are constructed as follows:

Initial conditions are:

- x (0)=1, x(1)= x(2)=...= x (16)= x (17)=0.
- y(0)=y(1)= ... =y(16)= y(17)=1.

Recursive definition of subsequent symbols are given as:

- x(i+18) =x(i+7) + x(i) modulo 2, i=0,...,2^{18}-20.
- y(i+18) = y(i+10)+y(i+7)+y(i+5)+y(i) modulo 2, i=0,..., 2^{18}-20.

The nth Gold code sequence z_n, n=0,1,2,...,2^{18}-2, is then defined as

$$z_n(i) = x((i+n) \text{ modulo } (2^{18} - 1)) + y(i) \text{ modulo } 2, \quad i=0,\ldots, 2^{18}-2$$

These binary sequences are converted to real valued sequences Z_n by the following transformation:

$$Z_n(i) = \begin{cases} +1 & if\ z_n(i) = 0 \\ -1 & if\ z_n(i) = 1 \end{cases} \quad for \quad i = 0,1,K\ ,2^{18} - 2.$$

Finally, the nth complex scrambling code sequence $S_{dl,n}$ is defined as:

$S_{dl,n}(i) = Z_n(i) + j\ Z_n((i+131072)\ \text{modulo}\ (2^{18}-1)),\ i=0,1,\ldots,38399.$

4.3.5 Combining downlink channels

After all downlink channels are scrambled, each downlink channel is weighted by appropriate weighting factors. All the downlink channels are then combined using complex addition as shown in Figure 4.7.

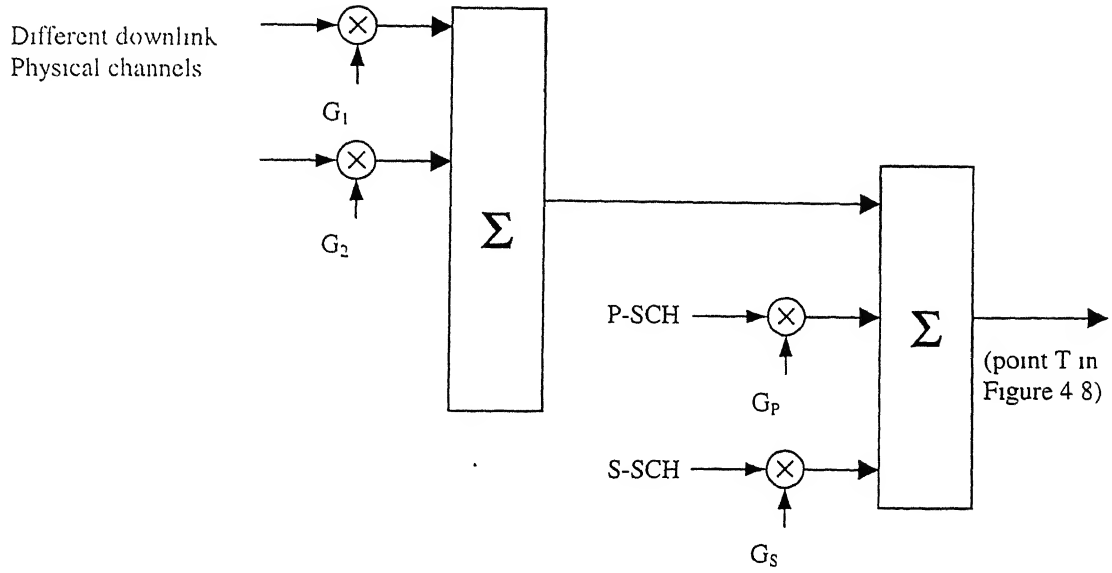


Figure 4.7: Complex addition of all downlink physical channels

4.3.6 Modulation

The complex valued chip sequence obtained by complex addition of all downlink channels is split into real and imaginary parts. The chips of real and imaginary parts are

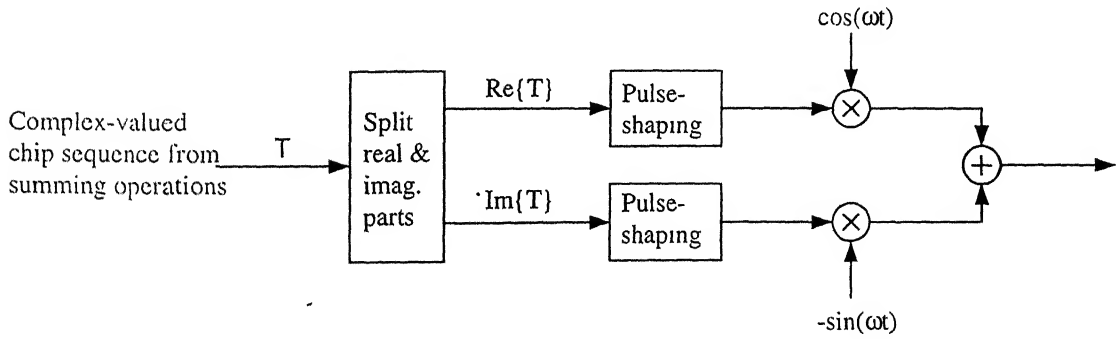


Figure 4.8: Downlink modulation

pulse shaped and QPSK modulated as shown in Figure 4.8. The modulated chips are combined into a complex sequence and transmitted. The modulating chip rate is 3.84 Mcps.

All the chapters till now have discussed concepts of software radios, structure of downlink channels and physical layer operations of downlink channels of WCDMA system Now we move over to implementation aspects. The software implementation details of all the downlink channels are given in next chapter. Last chapter gives the estimated computational requirements of the downlink channels.

Chapter 5

Implementation details of downlink physical channels

This chapter describes the implementation details of all downlink channels of WCDMA base station operating in FDD mode. Implementation details mean mapping of data on transport channels from MAC onto physical channels by performing physical layer operations as described in previous chapters. In order to estimate the computational requirements for implementing each physical channel, all the physical layer operations for each of the physical channels are implemented in software and are executed on a PC for a specific number (N) of frames. The percentage CPU required be taken as performance metric and is defined as the time taken to process N frames divided by the time during which those N frames have to be actually transmitted. In order to express the computational power in a processor independent way, SPEC benchmarks are chosen which expresses each of the commercially available processors computational power in SPEC ratings. The SPEC ratings for all current processors are given in [23]. By expressing the computational requirements of each channel in terms of SPEC ratings, the computational power required by each channel on future generation processors can be calculated.

5.1 Various downlink channels

The different downlink transport channels are

1. Speech channel.
2. 64 kbps data channel.
3. Simultaneous speech and 64 kbps data channels.
4. 144 kbps channel.
5. Simultaneous speech and 144 kbps data channels.
6. 384 kbps channel.
7. Simultaneously speech and 384 kbps data channels.

8. 2 Mbps channel for indoors and at pedestrian speeds.
9. ISDN channel.
10. Modem/Fax channel.
11. Common packet data channels such as Forward access channel (FACH) and Downlink shared channel (DSCH).
12. Control channels such as pilot channel, paging channel, synchronisation channel and indicator channels.

All these transport channels are mapped onto physical channels as described in previous chapters, by performing CRC coding, Channel Coding, Interleaving, Rate matching, Spreading and Scrambling. All these physical layer operations on all the listed channels listed above, are implemented in C language in this thesis for estimating the computational requirements of all downlink physical channels on a general purpose processor. All dedicated downlink transport channels are mapped onto dedicated physical channel (DPCH). Implementation procedure of all downlink dedicated data channels (1 to 10 in the list above) is identical except for difference in block lengths, transmission time intervals, SF etc. In next section, implementation details of speech and 64/144/384 kbps (3, 5, and 7 in above list) channel are given in detail for illustration and the procedure is identical for all other data channels. Implementation details of common packet channels (11) and control channels (12) are also given. Complete details for all channels are given in detail in [24].

5.2 Implementation details of Speech and 64/144/384 kbps channel

In WCDMA a user can have speech channel as well as 64/144/384 kbps data channel simultaneously. Following operations are performed in mapping speech and 64/144/384 kbps channel onto Dedicated Physical Channel (DPCH).

Adaptive Multi Rate (AMR) speech codec delivers speech at 12.2 kbps rate It outputs 244 or 39 or 0 bits for every 20 ms depending upon speech activity. Each output is divided into three blocks say TrCH #a, TrCH #b, TrCH #c and each block in individually coded. 244 bit output is split into three blocks of 81,103,60 bits, 39 bit output into 39,0,0 bit blocks and all 0 sized output into of 0 bit blocks as shown in Figure 5.1. After fragmenting each output into three blocks, 12 bit CRC coding is applied to the

first block. Rate 1/3 Convolutional coding (CC) is applied to CRC coded first block and to the uncoded second block, while CC of rate 1/2 is applied to uncoded third block. 8 tail bits are added to each block before convolutional coding. Tail bits are set as 0 and are used to clear the convolutional coder after encoding each block. All these parameters for speech channel are given in Table 5.1. The remaining part of Figure 5.1 is discussed later in this section.

For the data channel of 64/144/384 rate, data blocks of fixed size of 336 bits (including MAC overhead of 16 bits) arrives from the MAC layer every 20 ms (TTI). For 64 kbps channel, number of blocks for each TTI can be anyone of 0,1,2,4. For 144 kbps channel they can be any one of 0,1,2,4,8,9 and for 384 kbps channel they can be any one of 0,1,2,4,8,12,24. Each block is 16 bit CRC coded and all blocks are serially concatenated into a code block. Turbo coding is applied to the code block as shown in Figure 5.2. The block size input to Turbo coder cannot be more than 5114 (from section 4 1.2). For 384 kbps channel for the case of 24 input blocks, the size of code block is 8448 (greater than 5114). Code block segmentation is done for this case resulting in 2 code blocks. First block is filled with filler bits to make both blocks of equal size. Filler bits are set as 0. All the parameters of the data channel are given in Table 5.2. The remaining part of Figure 5.2 is discussed later in this section.

Table 5.1: Parameter for 12.2 kbps speech data

The number of TrChs		3
Transport block size	TrCH#a	N_{TrCHa}=0, 39 or 81bits
	TrCH#b	N_{TrCHb}=0 or 103 bits
	TrCH#c	N_{TrCHc}=0 or 60 bits
Possible output configurations	#1	N_{TrCHa}=81, N_{TrCHb}=103, N_{TrCHc}=60 bits
	#2	N_{TrCHa}=39, N_{TrCHb}=0, N_{TrCHc}=0 bits
	#3	N_{TrCHa}=0, N_{TrCHb}=0, N_{TrCHc}=0 bits
CRC		12 bits (attached only to TrCh#a)
Coding		CC, rate = 1/3 for TrCh#a, b Rate = 1/2 for TrCh#c
TTI		20 ms

Number of input blocks on data channel varies in each TTI. In order to convey number of blocks and the SF used a dedicated control channel (DCCH) at 3.4 kbps rate is multiplexed and transmitted along with speech and data channel. MAC delivers 148 bits (including MAC overhead of 12 bits) of DCCH for every 40 ms duration. This block is

16 bit CRC coded then convolutional coded (rate 1/3) as shown in Figure 5.3. All these parameters are shown in Table 5.3. The remaining part of Figure 5.3 is discussed later.

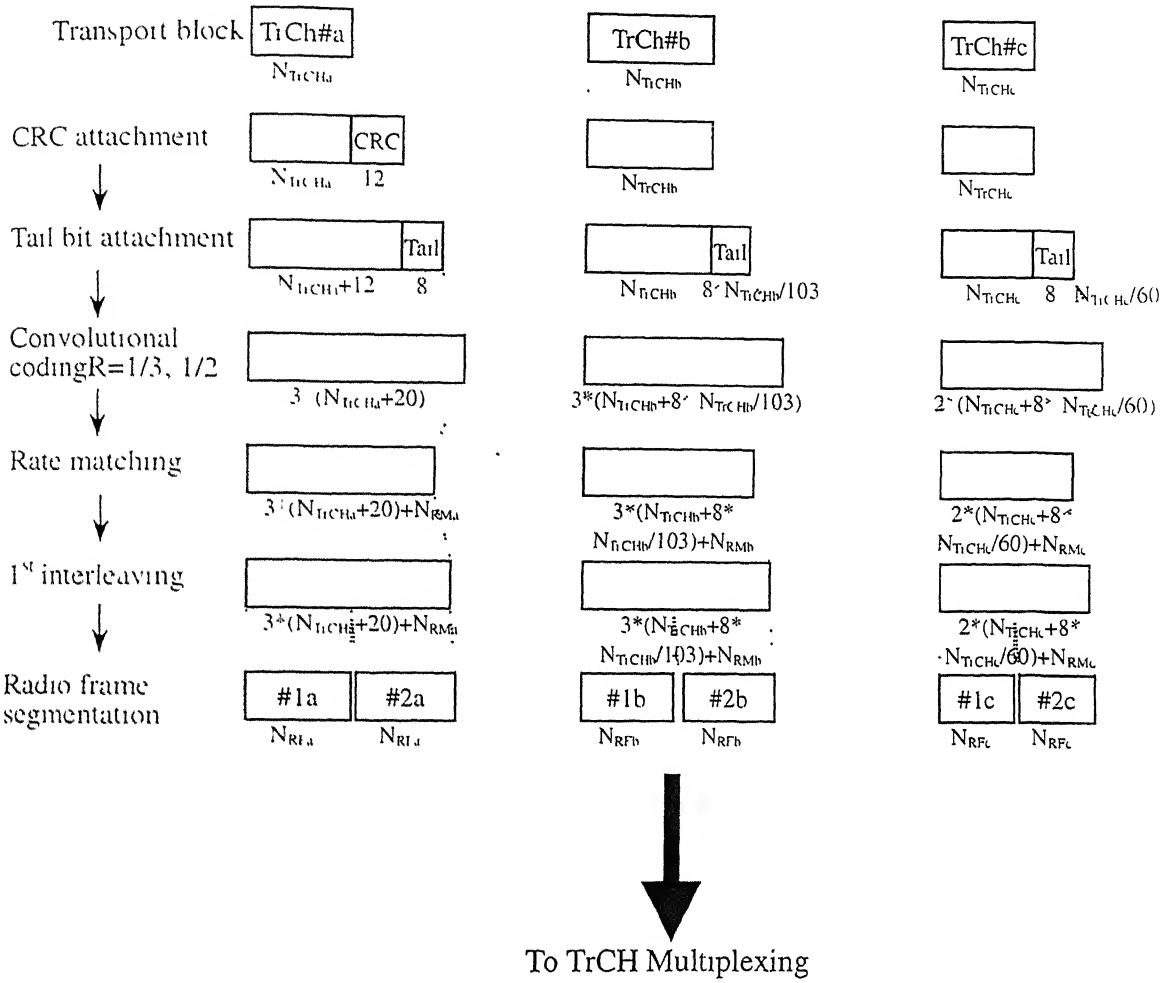


Figure 5.1: Channel coding and multiplexing 12.2 kbps AMR speech data

N_{TrCHa} = Number of bits on TrCH #a.

N_{TrCHb} = Number of bits on TrCH #b.

N_{TrCHc} = Number of bits on TrCH #c.

N_{RMa} = Number of bits of TrCH #a that are rate matched.

N_{RMb} = Number of bits of TrCH #b that are rate matched.

N_{RMc} = Number of bits of TrCH #c that are rate matched.

N_{RFa} = Number of bits on radio frame of TrCH #a.

N_{RFb} = Number of bits on radio frame of TrCH #b.

N_{RFc} = Number of bits on radio frame of TrCH #c.

16 CRC coded then convolutional coded (rate 1/3) as shown in Figure 5.3. All these parameters are shown in Table 5.3. The remaining part of Figure 5.3 is discussed later.

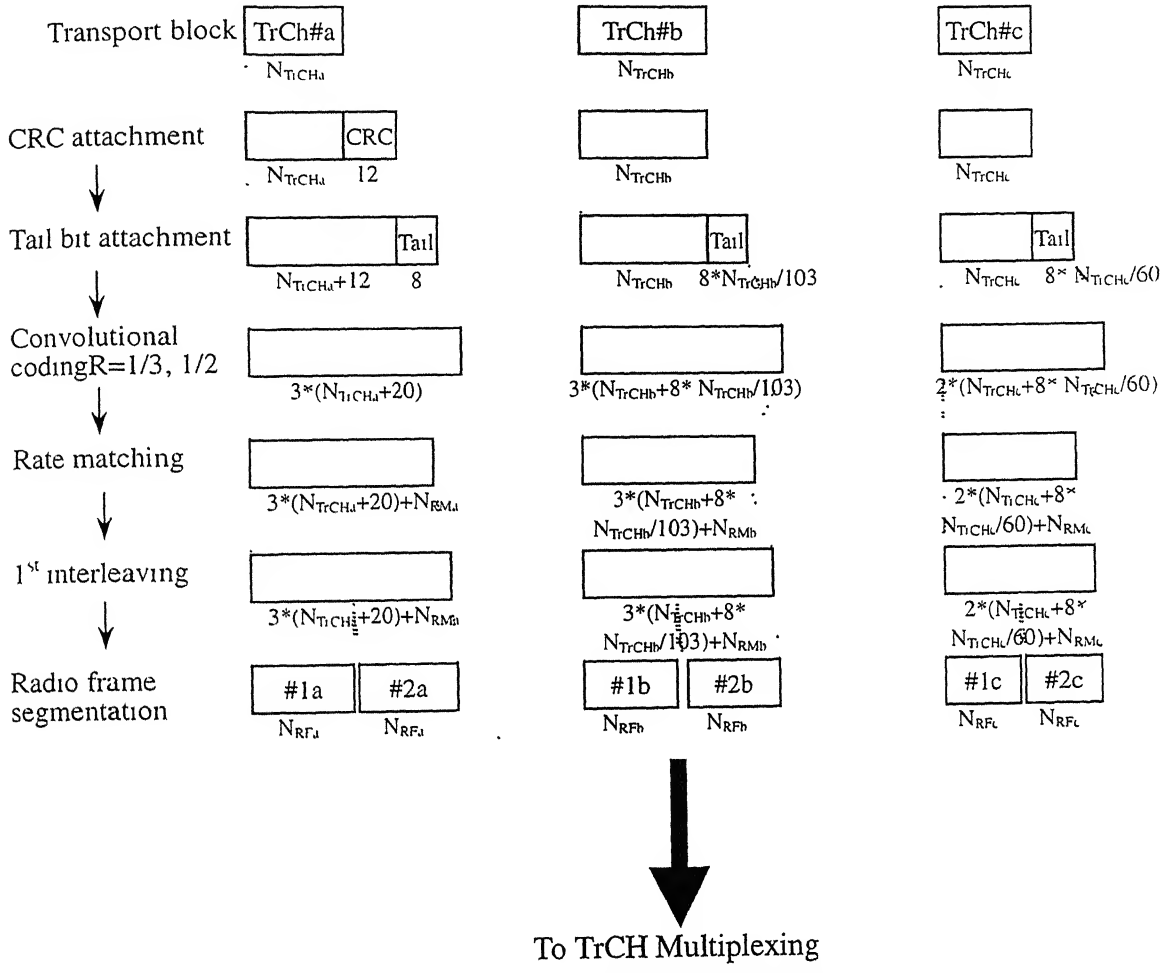


Figure 5.1: Channel coding and multiplexing 12.2 kbps AMR speech data

N_{TrCHa} = Number of bits on TrCH #a.

N_{TrCHb} = Number of bits on TrCH #b.

N_{TrCHc} = Number of bits on TrCH #c.

N_{RMa} = Number of bits of TrCH #a that are rate matched.

N_{RMb} = Number of bits of TrCH #b that are rate matched

N_{RMc} = Number of bits of TrCH #c that are rate matched.

N_{RMa} = Number of bits on radio frame of TrCH #a.

N_{RMb} = Number of bits on radio frame of TrCH #b.

N_{RMc} = Number of bits on radio frame of TrCH #c.

B = Number of Transport blocks per TTI.

Table 5.2: Parameters for 64/144/384 kbps packet data

Transport block size		336 bits
Transport block Set size	64 kbps	336*B bits (B = 0, 1, 2, 4)
	144 kbps	336*B bits (B = 0, 1, 2, 4, 8, 9)
	384 kbps	336*B bits (B= 0, 1, 2, 4, 8 , 12, 24)
CRC		16 bits
Coding		Turbo coding, coding rate = 1/3
TTI		20 ms

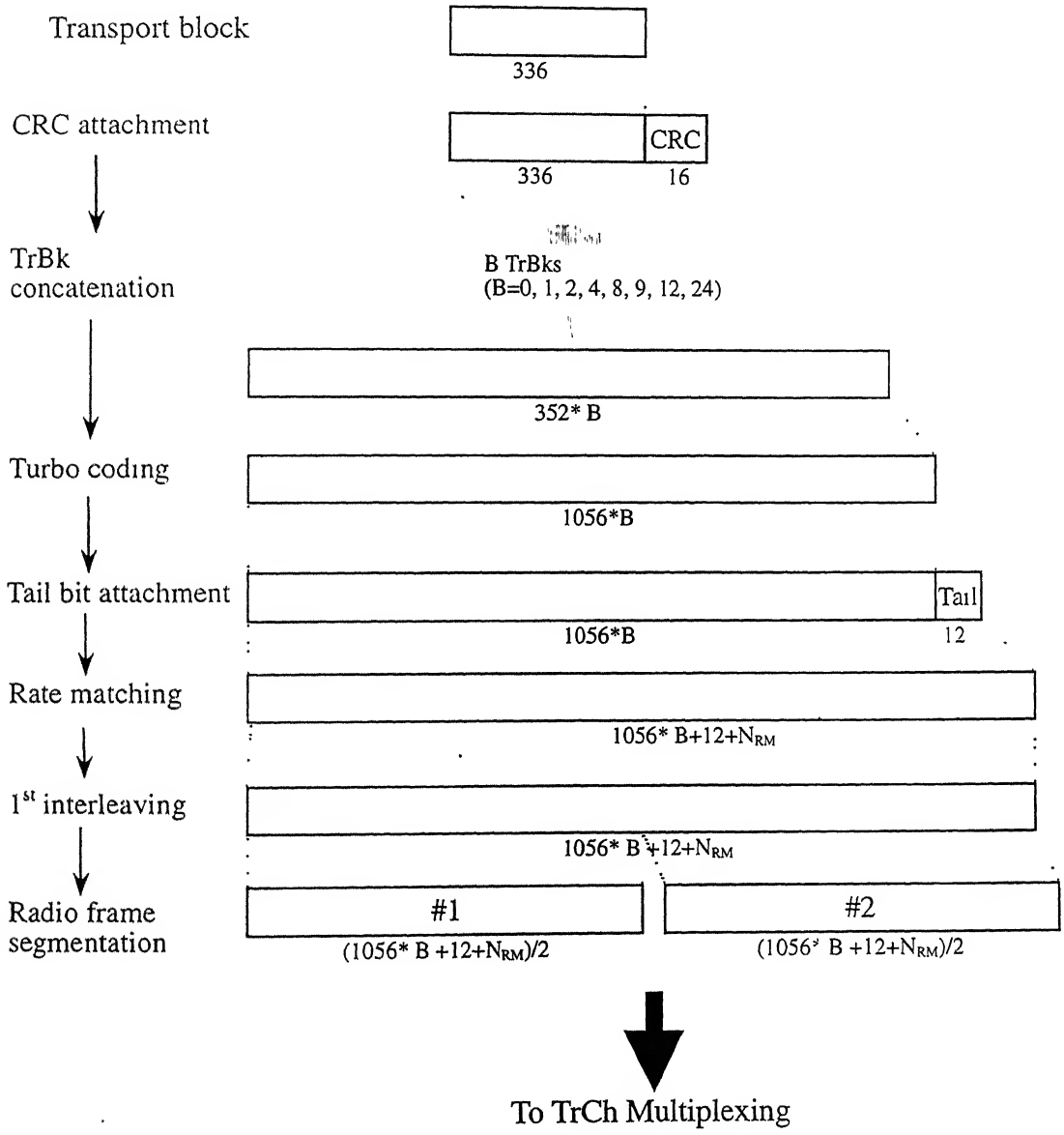


Figure 5.2: Channel coding and multiplexing of 64/144/384 kbps packet data

N_{RM} = Number of rate matched bits.

B = Number of Transport blocks per TTI.

Table 5.3: Parameter examples for 3.4 kbps DCCH data

Transport block size	148 bits
CRC	16 bits
Coding	CC, coding rate = 1/3
TTI	40 ms

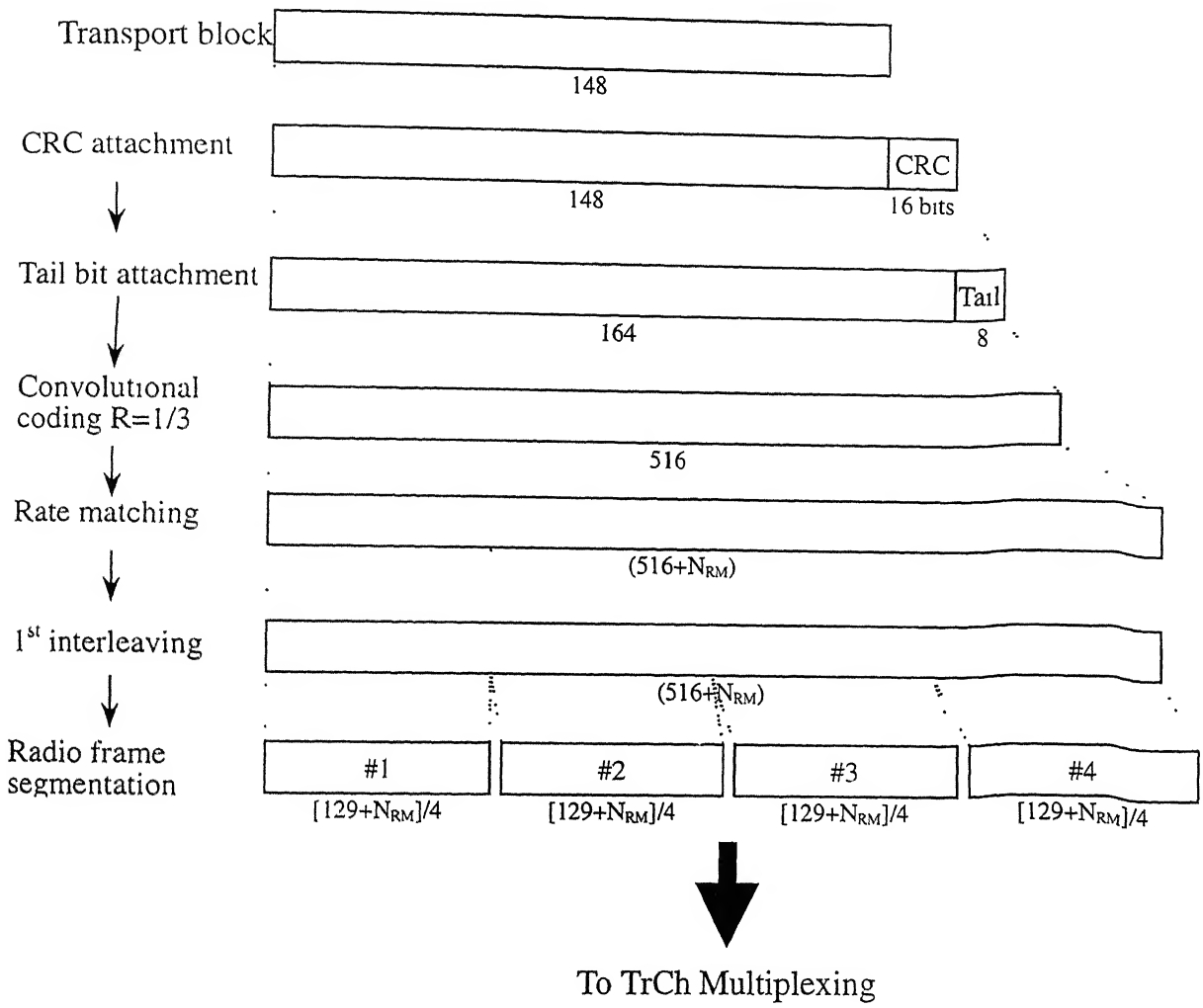


Figure 5.3: Channel coding and multiplexing of 3.4 kbps data

N_{RM} = Number of rate matched bits

All bits of speech, data (64/144/384 kbps) and DCCH are to be mapped onto dedicated physical channel (DPCH) that has fixed number of slots. As the number of bits of the speech and data channel varies for every TTI, bits have to be punctured or repeated so that they fit exactly on DPCH slots, called as Rate matching. Spreading factor (SF) is selected during Rate matching as explained later in this section.

For e.g. for 64 kbps channel with 4 transport blocks per TTI, the concatenated block size after CRC coding and Turbo coding is 4236 bits. For the speech channel assuming full speech activity (with 81,103,60 bit input blocks) number of bits per TTI (20 ms here) after CC is 303,333,136. For DCCH number of bits for each TTI (40 ms here) after CRC and convolutional coding is 516. As TTI of DCCH is 40 ms and TTI of speech and data channels is 20 ms, two successive frames of speech channel are concatenated so that they can be multiplexed with DCCH. For the same reason two successive frames of 64 kbps data channel are also concatenated. A total of 10532 bits containing 8472 bits of 64 kbps data channel (4236 Turbo coded bits for each 20 ms), 1544 bits of speech channel (772 convolutional coded bits for 20 ms) and 516 convolutional coded bits of DCCH should be transmitted for every 40 ms duration. 38400 chip slots on I channel and 38400 chip slots on Q channel are available for 10 ms on DPCH after spreading. A total of 307200 (2*38400*4) slots are available for 40 ms. 10532 bits of all transport channels (speech, 64 kbps data and DCCH) are to be mapped onto these available 307200 slots. A Spreading factor of 32 is preferred as 307200/10532=29.16. DPCH of 10ms duration is divided into 15 slots For SF of 32, 160 bit positions are available in each slot. Among them 140 are used for transport channels data and 20 are used for layer 1 control bits. With 15 slots for every 10 ms frame the total number of available slots for 40 ms duration is 60. Out of the available 9600 bit positions (160*60) for 40 ms duration, 8400 (140*60) are used for transport channel data and remaining 1200 (20*60) are used for layer 1 control bits. A total of 10532-8400=2132 bits of all data channels should be punctured (layer 1 control bits are not punctured). Puncturing is done individually on bits of each channel using the Rate matching algorithm given in section 4.1.6. After rate matching, bits of each channel are interleaved (first interleaving) as shown in Figures 5.1, 5.2, and 5.3. Interleaved bits of all data channels are segmented into 4 frames each of 10 ms time interval. DCCH data is segmented into 4 frames whereas each speech and data channel into 2 frames. First 10 ms frame of first speech channel, first 10 ms frame first data channel and first 10 ms frame of DCCH are serially concatenated into 10 ms duration frame of length 2100 bits, known as TrCH multiplexing as shown in Figure 5.4. Second interleaving is performed on each 10 ms frame. As each 10 ms duration of DPCH contains 15 slots, Interleaved frame of 2100 bits is split into 15 parts of 140 bits each. 140 data bits are multiplexed with 20 layer 1

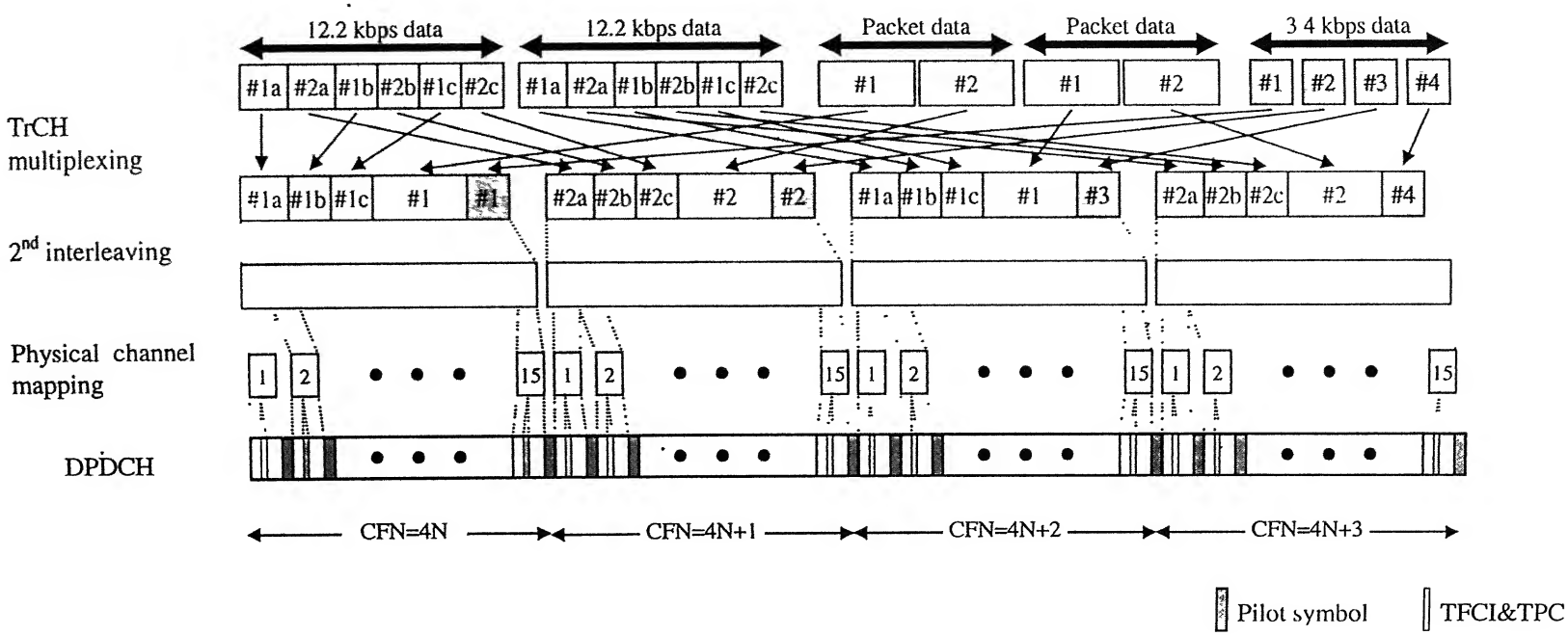


Figure 5.4: Multiplexing of 12.2 kbps speech data, 64/144/384 kbps packet data and 3.4 kbps DCCH data

Table 5.4: Physical channel parameters for multiplexing of 12.2 kbps speech, 64/144/384 kbps packet and 3.4 kbps DCCH data

Data rate (kbps)	Symbol rate (ksps)	N_{pilot} (bits)	N_{TFCI} (bits)	N_{TPC} (bits)	N_{data1} (bits)	N_{data2} (bits)
64	120	8	8	4	28	112
144	240	16	8	8	56	232
384	480	16	8	8	120	488

control bits and mapped onto each slot of DPCH. The number of control and data bits mapped onto each DPCH slot is given in Table 5.4.

Each pair of consecutive bits on DPCH are serial to parallel converted and mapped onto I and Q channels as shown in Figure 4.6. Bits on both branches are spread by same OVSF code. The chips on I and Q channels are combined into a complex sequence. The resulting complex sequence is scrambled by multiplying with a complex valued scrambling code as explained in section 4.3.

In the same manner all other downlink channels are mapped onto DPCH. A brief explanation of mapping of all other downlink channels onto DPCH is given later in this section and was given in detail in [24].

5.3 Implementation details of other channels

For speech channel, the procedure of mapping of AMR speech codec bits and DCCH bits onto DPCH is identical to that of speech and 64/144/384 data channel but without 64/144/384 kbps data channel. The SF used is 128.

For 64/144/384 channel, the procedure of mapping 64/144/384 kbps data channel and DCCH bits onto DPCH is identical to that of speech and 64/144/384 kbps channel without speech channel.

For 2 Mbps channel, MAC delivers 256 blocks of size 336 bits once every 40 ms (TTI). Each input block is 16 bit CRC coded and all blocks are concatenated. As input block size to Turbo coder cannot be more than 5114 bits, the concatenated block is segmented into 18 code blocks of size 5114 each with first block filled with filler bits Filler bits are set to 0. Each segmented code block is Turbo coded and all turbo-coded blocks are serially concatenated, then Rate matched, interleaved (First interleaving) and segmented into 4 frames each of 10 ms duration. DCCH data of size 148 bits are CRC coded, convolutional coded (rate 1/3), Rate matched and interleaved (first interleaving). Interleaved bits of DCCH are segmented into 4 frames of 10 ms duration each. First 10 ms duration frame of 2 Mbps channel is serially concatenated with the first 10 ms duration frame of DCCH and all other three frames are also multiplexed in the same way, called as TrCH multiplexing. The multiplexed frame is interleaved (Second interleaving) again over its 10 ms duration. As data rate is very high, single physical channel cannot transmit all the bits. Thus three DPCHs are used in parallel each with different

coded and others are Turbo coded. Then bits on all the channels are Rate matched, interleaved (first interleaving) and TrCH multiplexed. The resulting bits are mapped onto SCCPCH slots multiplexed with layer 1 control bits. Each pair of consecutive bits are mapped onto I and Q channels and bits on both channels are spread by using same channelisation code. The chips on both I and Q channels combined into a complex sequence. A complex scrambling code scrambles the resulting complex chip sequence. Length of the channelisation code used varies from 256 to 4 depending upon number of FACHs and number of bits on each FACH.

Mapping of DSCH onto PDSCH is identical to that of mapping PCH and FACH onto SCCPCH. Many DSCHs are mapped onto PDSCH and SF is varied from 256 to 4 depending upon the number of DSCHs and amount of data on each DSCH.

Pilot channel transmits a predefined symbol sequence. Alternate bits of the predefined symbol sequence are mapped onto I and Q channels and bits on I and Q channels are spread by the same channelisation code of length 256. The chips on I and Q channels are combined into a complex sequence. The resulting complex valued chip sequence is scrambled by multiplying with a complex valued scrambling code.

Paging indicators generated by higher layers for a UE are mapped onto paging indicator channel (PICH). 288 paging indicator bits and 12 bit positions with no transmission are mapped onto PICH for every 10 ms. Each pair of bits are mapped onto I and Q channels. Bits on both I and Q channels are spread by using same channelisation code of length 256. The chips on I and Q channels are combined into a complex sequence. A complex scrambling code scrambles the resulting complex chip sequence.

Indicator channels (ICHs) carry indicator bits that correspond to signatures on RACH and CPCH. Acquisition indicator channel (AICH), CPCH Access Preamble Acquisition Indicator channel (AP-AICH), CPCH Collision Detection/Channel Assignment Channel (CD/CA-ICH), CPCH Status Indicator Channel (CSICH) are the different indicator channels as explained in chapter 4. The frame format of all indicator channels is identical. Each indicator channel frame length is of 20 ms duration, divided into 15 slots. Each slot accommodates 20 real valued symbols (20 bits on I channel and 20 bits on Q channel). Each slot is divided into two parts with first part of length 16 symbols and second part of length 4 symbols. Indicator bits of all channels except for

CSICH are transmitted in first part while for CSICH they are transmitted in second part. 8 indicator bits of CSICH are mapped onto second part of slot while 32 indicator bits of all other ICHs are mapped onto first part of slot. The other part of all ICHs that are without indicator bits is with no transmission. All 15 slots of frame are filled with indicator bits in same manner. Each pair of bits on ICHs are mapped onto I and Q channels. Bits on I and Q channels are spread using same channelisation code of length 256 and combined into a complex sequence. A complex scrambling code scrambles the resulting complex chip sequence.

Scrambled chip sequences of all downlink channels are weighted by weighting factors and are combined using complex addition as shown in Figure 4.7

Chapter 6

Results and discussion

This chapter gives the computational power required for realizing each downlink physical channel of 3G WCDMA base station. The computational power required for realizing all downlink channels in a typical base station has been evaluated. The computational power required by each downlink channel is expressed in terms of %CPU required on Intel Pentium III 450 MHz processor and also in terms of SPEC95 ratings [23]. SPEC95 ratings are expressed with two sub components, 'SPEC int 95' focusing on integer/non floating-point compute intense activity and 'SPEC fp 95' focusing on floating point compute intense activity. Three different systems each with varying number of various downlink channels are considered and computational complexity for each system is calculated. The computational requirements of the three systems gives an estimate of the computational requirements of downlink (forward link) in practical real time base stations. The computational power in %CPU metric for each channel is calculated as follows. All physical layer operations of each channel that are implemented in software are executed on a PC for N frames. The time taken to process these N frames is divided by the time duration in which those N frames have to be actually transmitted gives %CPU metric. The fractional CPU usage is obtained by dividing %CPU metric by 100. SPEC ratings are obtained by multiplying the fractional CPU usage with the SPEC rating of the Pentium III 450 MHz processor as given in Table 6.4.

6.1 Computational requirement of forward link channels in WCDMA base station

Table 6.1 gives the computational requirements of all the downlink channels in terms of % CPU metric and in SPEC 95 ratings.

Table 6.1: Downlink channels performance metrics

Physical Channel	Performance metric		
	% CPU	SPEC Ratings	
		SPEC int 95	SPEC fp 95
PCCPCH	2.178	0.41	0.30
SCCPCH	76.96	14.39	10.54
PDSCH	38.00	7.15	5.21
Modem/Fax channel	82.35	15 40	11 28
ISDN channel	84.05	15.72	11.51
Speech channel	54.90	10 27	7.52
64 kbps data ch.	84.90	15.88	11.63
144 kbps data ch	109.83	20.54	15.05
384 kbps data ch.	158.42	29.62	21.7
Speech & 64 kbps ch.	107.55	20 11	14.73
Speech & 144 kbps ch.	153.70	28.74	21.06
Speech & 384 kbps ch.	243.59	45.55	33.37
2 Mbps data rate ch.	1452.13	271.55	198.94
Sync. Channel	7.364	1.38	1.01
AICH or AP- AICH or CD/CA-AICH	130.20	24.35	17.84
CPICH	52.68	9.85	7.22
CSICH	4.96	0.93	0.68
PICH	47.92	8.96	6.57

WCDMA uses RF carriers of 5 MHz bandwidth each. With 60 MHz of allocated bandwidth for downlink of WCDMA, 12 RF carriers each of 5 MHz are available. On each 5 MHz RF carrier 128 Speech channels or thirty two 64 kbps data rate channels can be transmitted depending on the SF of channel (SF of Speech channel is 128, SF of 64 kbps channel is 32). The number of channels that can be transmitted on single RF carrier is equal to SF of the channel [21]. For a base station, assuming a frequency reuse factor of 1 (Ideal case) and without any sectorisation 12 RF carriers are available. The available

12 carriers can support different number of different types of downlink channels (speech, 64 kbps data rate, 144 kbps data rate etc). Three systems are considered each with different number of different types of channels. We classify these as System I, II, and III. System I correspond to equal number of voice and data channels System II corresponds to 60% voice channels and 40% data channels. System III corresponds to 40% voice channels and 60% data channels. The three systems that are considered represents the traffic requirements in real time base stations.

Table 6.2 gives the number of different downlink channels assumed for three systems with RF carriers onto which they are mapped.

Table 6.2: Number of channels supported on each RF carrier for different systems

RF Carrier	Type of channel	No. of channels supported		
		System I	System II	System III
1	64 kbps data rate ch.	32	32	32
2	Speech & 64 kbps	32	32	32
3	144 kbps data rate ch.	16	16	16
4	Speech & 144 kbps	16	16	16
5 , 6	2 Mbps data rate ch.	2	2	2
	384 kbps data rate ch.	4	4	4
7	Control and Indicator	32	32	32
	Speech channel	40	96	-
	64 kbps data rate ch.	5	-	12
	Speech & 64 kbps	5	-	12
	384 kbps data rate ch.	2	1	1
8	Speech channel	128	128	128
9 , 10	Speech channel	-	16	-
	ISDN	16	16	16
	Modem/Fax	16+16	16+16	24+16
	Speech & 384 kbps	6	5	5
11	SCCPCH	32	32	32
12	PDSCH	16	16	16

For system I the allocation of RF carriers to the different downlink channels is explained below and it is identical for the other two systems. The mapping of different channels of different SF onto different RF carriers is described as below

In order to transmit physical channels of variable data rates on the same carrier, spreading codes with different spreading factors (SFs) are to be used. Two channels that are spread with different length spreading codes are orthogonal if and only if the spreading codes used by one channel is not derived from the code used by other channel. In Figure 4 5, spreading (channelisation) code $C_{ch,4,0}$ is derived from the code $C_{ch\,2,0}$. So two channels that are spread by $C_{ch,4,0}$ and $C_{ch,2,0}$ are not orthogonal. So these codes cannot be assigned to different physical channels of same carrier. In the same way if $C_{ch,2,0}$ is assigned to one channel all the codes that are derived from it i.e. $C_{ch,4,0}$, $C_{ch,4,1}$, $C_{ch,8,0}$, $C_{ch,8,1}$, $C_{ch,8,2}$, $C_{ch,8,3}$, $C_{ch,16,0}$ ..... $C_{ch,16,7}$ .. should not be assigned to any other physical channels as they cannot be orthogonal. In this way consider the mapping of 2Mbps channel and 384 Kbps channels onto carriers 5 and 6 of Table 6.2. One 2 Mbps channel needs 3 spreading codes (physical channels) each of SF 4. To transmit two 2 Mbps channels 6 codes (physical channels) each of SF 4 each are needed. One carrier can transmit 4 physical channels each of SF 4. Both carriers can transmit 8 physical channels each of SF 4. Out of available 8 codes on both carriers 6 are used to transmit both 2 Mbps channels. The spreading codes that can be derived from these 6 assigned codes cannot be assigned to any other channels as they cannot be orthogonal with the codes assigned to 2Mbps channels. From the remaining 2 codes of length 4 each, 4 codes each of length 8 are derived. As SF of each 384 Kbps channel is 8, four 384 Kbps channels are transmitted on the available 4 codes of length 8 each. In the same way different physical channels are assigned to different carriers.

For system I the mapping of different downlink physical channels to RF carriers is as follows. First RF carrier is used to transmit 32 channels of 64 kbps data rate each of SF 32. 32 channels of speech and 64 kbps data channel of SF 32 are transmitted on second RF carrier. Third RF carrier is used to transmit 16 channels of 144 kbps data rate channel each of SF 16, fourth carrier is used to transmit 16 channels of speech and 144 kbps data rate each of SF 16. One RF carrier can transmit 4 physical channels each of SF 4. In order to transmit one 2 Mbps channel, 3 physical channels i.e. 3 channelisation

codes are needed. Out of 8 channelisation codes of SF 4 available on fifth and sixth carriers, 6 codes are used to transmit two 2 Mbps data rate channels. Remaining 2 codes of SF 4 i.e. 4 codes of SF 8 are used to transmit four 384 kbps data rate channel of SF 8. Out of 256 channelisation codes of length 256 available on seventh RF carrier, 32 codes are used to transmit 32 control and indicator channels (BCH, Pilot, AICH, AP-AICH, CD/CA-ICH, CSICH, PICH) each with SF 256. With the remaining 224 codes of SF 256 i.e 112 codes of SF 128, 40 codes are used to transmit 40 speech channels each of SF 128. On the same carrier, with the remaining 72 codes of SF 128 i.e. 36 codes of SF 64 i.e 18 codes of SF 32, five codes are used to transmit 64 kbps data rate channel each with SF 32 and 5 more codes are used to transmit speech & 64 kbps channel each of SF 32. On the same carrier, with remaining 8 codes of SF 32 i.e. 4 codes of SF 16 i.e. 2 codes of SF 8 two 384 kbps data rate channels each of SF 8 are transmitted. Eighth RF carrier is used to transmit 128 speech channels each of SF 128. Ninth RF carrier is used to transmit 16 ISDN channels of SF 32 each and 16 Fax data channels of SF 32 each. Out of available 64 codes of SF 64 on tenth RF carrier, 16 codes are used to transmit 16 Modem data channels each of SF 64. On the same carrier with remaining 48 codes of SF 64 i.e. 24 codes of SF 32 i.e. 12 codes of SF 16 i.e. 6 codes of SF 8, all 6 codes are used to transmit 6 speech and 384 kbps data rate channels of SF 8 each. With two remaining RF carriers (eleventh and twelth), one is used to transmit SCCPCH and other is used for PDSCH. Out of 32 channelisation codes assigned to control and indicator channels, 2 codes are used for control channels i.e. for common pilot channel and Broadcast channel and remaining 30 codes are used for indicator channels as follows. 6 codes for AICH, 6 codes for AP-AICH, 6 codes for CD/CA-ICH, 6 codes for CSICH and 6 codes for PICH.

In the same way, different downlink channels can be mapped onto different RF carriers for each system as shown in Table 6.2.

By assuming speech & 64 kbps data rate channel, speech & 144 kbps data rate channel, speech & 384 kbps data rate channel as data channels and with out considering common data channels, the number of voice channels, data channels (irrespective of data rates) and total number of channels supported by each system is shown in Table 6.3.

Table 6.3: Number of downlink channels supported by each system

	System 1	System 2	System 3
No. of voice channels	**168**	**240**	**128**
Speech ch.	168	240	128
No. of data channels	**168**	**156**	**187**
64 kbps data rate ch.	37	32	44
144 kbps data rate ch.	16	16	16
384 kbps data rate ch	6	5	5
Speech & 64 kbps	37	32	44
Speech & 144 kbps	16	16	16
Speech & 384 kbps.	6	5	5
2 Mbps data rate ch.	2	2	2
Modem/Fax	16+16	16+16	24+16
ISDN channel	16	16	16
Total No. of channels	**336**	**396**	**315**

The computational power required for all downlink physical channels of three systems is given in Table 6.5 in terms of SPEC ratings The total computational power required by three systems is also given. By using the SPEC ratings of some processors as shown in Table 6.4, the number of Intel Pentium III processors at 1 GHz required to realize each system is around 150 and is given in detail in Table 6.6. This value is indicating the huge computational power required to realize the downlink of software based WCDMA base station. It seems that with the present processor technology it may not be possible to practically realize software based 3G WCDMA base station.

Table 6.4: SPEC95 Ratings.

Platform	Clock	SPEC int 95	SPEC fp 95
Intel Pentium III	450 MHz	18.7	13.7
Intel Pentium III	1 GHz	46.8	32.2

Table 6.5: Downlink channels performance metric in SPEC ratings

Channel Type	System I		System II		System III	
	SPEC int 95	SPEC fp 95	SPEC int 95	SPEC fp 95	SPEC int 95	SPEC fp 95
PCCPCH	0.41	0.30	0.41	0.30	0 41	0.30
SCCPCH	460.48	337.28	460.48	337.28	460.48	337.28
PDSCH	114.40	83.36	114.40	83.36	114.40	83 36
Modem/Fax channel	492.80	360.96	492.80	360.96	616.00	451.20
ISDN channel	251.52	184.16	251.52	184 16	251.52	184.16
Speech channel	1725.36	1263.36	2464.80	1804 80	1314.56	962 56
64 kbps data ch.	587.56	430.31	508.16	372.16	698.72	511.72
144 kbps data ch.	328.64	240.80	328.64	240 80	328.64	240 80
384 kbps data ch	177 72	130.20	148.10	108.50	148.10	108.50
Speech & 64 kbps ch.	744.07	545.01	643.52	471.36	884 84	648.12
Speech & 144 kbps ch.	459.84	336.96	459.84	336.96	459.84	336 96
Speech & 384 kbps ch.	273.30	200.22	227.75	166.85	227.75	166.85
2 Mbps data channel	543.11	397.88	543.11	397.88	543.11	397.88
Sync. channel	1.38	1.01	1.38	1 01	1.38	1.01
Indicator channels	438.30	321.12	438.30	312 12	438.30	312 12
CPICH (Pilot channel)	9.85	7.22	9.85	7.22	9.85	7.22
CSICH	5.58	4.08	5.58	4 08	5.58	4.08
PICH (Paging ICH)	53.76	39.42	53.76	39.42	53.76	39.42
TOTAL	**6668.08**	**4883.65**	**7152.4**	**5229.22**	**6557.24**	**4793.54**

Table 6.6: Number of P III (1 GHz) processors required

	No. of processors required	
	Min	Max
System I	143	152
System II	153	163
System III	141	149

6.2 Conclusion

As software radio approach provides tremendous flexibility, in our present study we have aimed to investigate the possibility of realizing the WCDMA base station in software. Focusing on this, all downlink physical channels for 3GPP WCDMA base station system for FDD mode are implemented in software in C language. The computational power required for realizing each downlink physical channel has been given in terms of %CPU metric and in SPEC ratings. As %CPU metric depends upon the processor used, SPEC ratings are used to express computational power in platform independent way. By expressing the computational power in SPEC ratings, the computational required on future generation processors can be estimated. Three base station systems are assumed each with different downlink channels. Computational power required to realize the downlink channels for each system is presented inorder to get an estimate of the computational power required to realize a real time base station. From the results it has been observed that inorder to support around 350 users in downlink, 150 Pentium III processors running at 1 GHz are required. This is a quite high figure This high value is indicative of the conclusion that at present it is not possible to realize the downlink of WCDMA base station completely in software. With the availability of more powerful processors in future, it may be practically feasible to realize the downlink of WCDMA base stations in software with reasonable number of processors.

6.3 Future work

In this thesis the computational requirements of all downlink channels of WCDMA base station system are estimated. The results indicate a requirement of large number of processors to realize the system. In future, even with the availability of more powerful processors it may not be possible to realize the whole downlink on a single processor but can be implemented with a reasonable number of processors using structures such as MDNS as given in Chapter 2. In MDNS approach the distribution of processors to each PU can be studied in detail for optimum usage of number of processors. The computational power required by all uplink channels also needs investigation. By knowing the computational requirements of uplink, the whole computational requirements for software realization of 3G WCDMA base station can be estimated. For efficient spectrum usage multi-user detection techniques and adaptive antennas are being

considered by 3GPP group to incorporate into WCDMA system. The software realization of these features can be investigated. The dynamic allocation of channelisation codes to different RF carriers can also be studied.

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